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New tests and test methodologies for scan cell internal faults

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NEW TESTS AND TEST METHODOLOGIES FOR SCAN CELL INTERNAL FAULTS

by

Fan Yang

An Abstract

Of a thesis submitted in partial fulfillment of the
requirements for the Doctor of Philosophy degree
in Electrical and Computer Engineering
in the Graduate College of
The University of Iowa

December 2009

Thesis Supervisors: Professor Sudhakar M. Reddy
Sreejit Chakravarty

ABSTRACT

Semiconductor industry goals for the quality of shipped products continue to get higher to satisfy customer requirements. Higher quality of shipped electronic devices can only be obtained by thorough tests of the manufactured components. Scan chains are universally used in large industrial designs in order to cost effectively test manufactured electronic devices. They contain nearly half of the logic transistors in large industrial designs. Yet, faults in the scan cells are not directly targeted by the existing tests. The main objective of this thesis is to investigate the detectability of the faults internal to scan cells.

In this thesis, we analyze the detection of line stuck-at, transistor stuck-on, resistive opens and bridging faults in scan cells. Both synchronous and asynchronous scan cells are considered. We define the notion of half-speed flush test and demonstrate that such new tests increase coverage of internal faults in scan cells. A new set of flush tests is proposed and such tests are applied at higher temperatures to detect scan cell internal opens with a wider range of resistances. We also propose new scan based tests to further increase the coverage of those opens. The proposed tests are shown to achieve the maximum possible coverage of opens in transistors internal to scan cells. For an asynchronous scan cell considered, two new flush tests are added to cover the faults that are not detected by the tests for synchronous scan cells. An analysis of detection of a set of scan cell internal bridging faults is described. Both zero-resistance and nonzero-resistance bridging fault models are considered. We show that the detection of some zero-resistance non-feedback bridging faults requires two-pattern tests. We classify the undetectable faults based on the reasons for their undetectability.

We also propose an enhanced logic BIST architecture that accomplishes the new flush tests we propose to detect scan cell internal opens.

The effectiveness of these new methods to detect scan cell internal faults is demonstrated by experimental results using some standard scan cells from a large industrial design.

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Graduate College
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Iowa City, Iowa

CERTIFICATE OF APPROVAL

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PH.D. THESIS

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This is to certify that the Ph.D. thesis of

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has been approved by the Examining Committee
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To My Family

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ABSTRACT

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CHAPTER I INTRODUCTION

Semiconductor industry goals for the quality of shipped products continue to get higher to satisfy customer requirements. For example high end automobile manufacturers are requiring zero defects in the electronic components. Similar requirements are customary for life critical systems. Higher quality of shipped electronic devices can only be obtained by thorough tests of the manufactured components. **Testing** of Very Large Scale Integrated (VLSI) circuits is an experiment in which the circuits are exercised by a group of binary values to ascertain the correctness of circuit behaviors.

1.1 Design-for-test and scan design

Test complexity can be converted into costs associated with the testing process. It may be from the cost of test pattern generation, the cost of fault simulation and generation of fault location information, the cost of test equipment, and the cost related to the testing process itself called the time required to detect a fault [1.1]. **Testability** is a design characteristic that influences various costs associated with testing. **Design for testability** or design-for-test (DFT) methods are design efforts specifically employed to ensure that a device is testable.

Testable circuitry is both controllable and observable. The **controllability** is used to measure the difficulty of setting a line to a value. In order for the detection of a fault, fault propagation is required where primary inputs are set to appropriate values such that the fault is able to propagate to at least one of the primary outputs (i.e., one or more primary outputs present the faulty value due to the fault). The ability of fault propagation is measured by the **observability** which indicates the relative difficulty of propagating an error from a line to a primary output. In a testable design, setting specific values on the primary inputs results in values on the primary outputs which indicate whether or not the internal circuitry works properly.

The most common DFT technique to increase the controllability and observability of a circuit is **scan design**, which modifies the internal sequential circuitry of the design. The digital circuits are classified into combinational logic and sequential logic. **Combinational circuit** outputs depend solely on the primary inputs, whereas **sequential circuit** outputs depend on stored values from previous time frame also the primary inputs. The goal of scan design is to make difficult-to-test sequential circuit behave like an easier-to-test combinational circuit during the testing process. In order to achieve this goal sequential elements are replaced with so called scan cells. These scan cells are then stitched together into scan chains. This process is demonstrated next refer to Figure 1-1.

The design shown in Figure 1-1 contains both combinational and sequential portions. In Figure 1-1(a), the values of functional data-in (Ds) in the memory elements are the state outputs from the combinational logic. These values are then transferred to Qs which are the inputs of the combinational logic in the next time frame. To initialize the states of the circuit in Figure 1-1(a) we may need back-tracking the states of the previous time frames. In addition, it may also require line justifications to propagate the errors. Hence, this “Before scan” circuit is difficult to initialize to a known state, making it difficult to both control the internal circuitry and observe its behavior using the primary inputs and outputs of the design. However, we may add the scan circuitry into the design to set the state variables and observe the state outputs directly.

Figure 1-1(b) has two additional inputs, scan-in (TI1) and scan enable (TE), and one additional output, Q(n+1). The scan cells replace the original memory elements so that scan data are shifted into the combinational logic from TI1 signal when TE is active. During the functional mode (normal operation), TE is deactivated. No values are read in from TIs in scan cells. Ds are selected to propagate to Qs. During the testing, the operating procedure is as follows:

(1) Enable the scan enable signal TE to allow shifting to initialize scan cells. This will load TIs with proper values.

(2) Turn off the scan clocks and apply primary inputs to the circuitry. The primary outputs and new values on Ds are set after this step.

(3) Pulse the clock to capture new values into scan cells.

(4) Finally, activate the TE signal to shift Qs out of the scan chain. The values at Q(n+1) are then compared with the expected values.

In the scan design, we can set input states and primary inputs. Besides, both state outputs and primary output are observed.

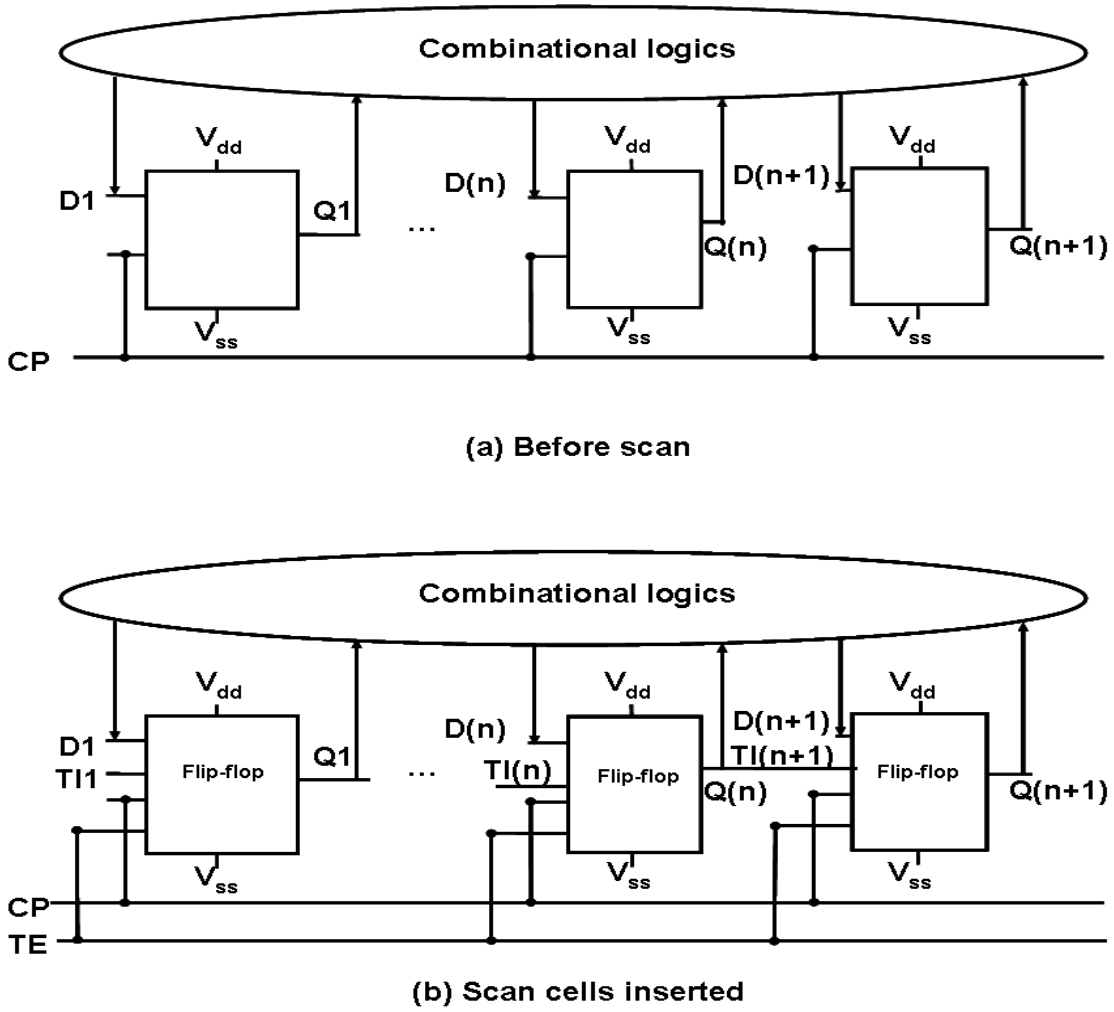


Figure 1-1: Scan design process

1.2 Overview of the thesis

Because of the rapid increase in the complexity of VLSI circuitry, the issue of testing and design-for-test are becoming increasingly more important. In order to cost effectively test manufactured electronic devices, scan design is universally used in industry. In full scan designs, all flip-flops in the logic part of a design are grouped into the scan chains that facilitate loading tests applied to detect defects as well as observing the circuit response to the tests. This requires augmenting the functional flip-flops into what are called scan flip-flops or scan cells. Even though the main purpose of scan cells is to facilitate loading tests and unloading test responses, faults in scan cells may affect functional operation if left undetected. This is because scan cells contain the functional flip-flops. The undetected faults in scan cells may also affect long term reliability of shipped products. Table 1-1 shows the gate and transistor counts of a 90nm industrial design we investigated. Approximately 14.3% of the logic cells are scan cells but they contain about 43.6% of the total number of transistors in the logic part of the design. Nevertheless, faults in the scan cells are not directly targeted and assumed detected by what are called flush tests. Thus, it is important to determine the coverage of faults internal to the scan cells and investigate cost effective methods to augment tests generated by standard automatic test pattern generation (ATPG) procedures to detect scan cell internal faults.

The assumptions made to represent the nature of logic faults are called **fault models**. Traditional fault models include stuck-at, stuck-on, stuck-open and bridging faults. In this thesis, we investigate the detectability of stuck-at, transistor stuck-on, transistor opens and shorts internal to scan cells by the existing tests which include flush tests and ATPG tool generated tests. This thesis investigates to develop new tests and methodologies to apply the tests to maximize the fault coverage.

1.3 Organization of the thesis

The rest of this thesis is organized in the following manner.

Chapter II gives an introduction of the structure of scan flip-flop and briefly reviews of the existing tests and some related previous work for testing of scan cells.

Chapter III presents results of the first step in the direction of investigating the use of standard scan cells and existing methods of generation and application of scan based tests to detect scan cell internal faults using stuck-at and stuck-on fault models. A new flush test, half-speed flush test, is proposed to enhance the detectability of those considered faults.

Chapter IV reports the detection of a set of scan cell internal bridging faults extracted from layout. A comprehensive analysis of bridging faults internal to scan cell is developed.

The detectability of large resistance opens in transistors internal to scan cells is investigated in Chapter V. New flush tests to maximize the fault coverage of those opens in a synchronous scan cell are described.

Chapter VI investigates the scan chain internal transistor opens with moderate resistances. The flush tests proposed earlier for the detection of large resistance opens internal to scan cells are modified to maximize the range of detectable open resistances. Application of flush tests at higher temperature to improve the range of open resistances detected is also discussed.

Chapter VII presents an enhanced logic BIST architecture for online testing. The new flush tests for opens internal to scan chains are augmented into the tests generated by the new logic BIST architecture.

In addition to synchronous scan cell considered, in Chapter VIII, an asynchronous scan cell is also studied and two new flush tests are added to cover the faults that are not detected by the tests for synchronous scan cell.

Finally, Chapter IX summarizes this thesis and describes some topics for future research.

Table 1-1: Gate and transistor data of an industrial design

	Combinational Gate	Latch	Scan Flip-Flop
# of Cells	3678245 (85.6%)	3256 (0.08%)	614159 (14.3%)
# of Transistors	30634354 (56.4%)	53588 (0.1%)	23670019 (43.5%)

CHAPTER II REVIEW OF TESTS AND METHODS FOR TESTING OF SCAN CELL

In this chapter we summarize the previous works on testing of scan cells. Specifically, in the first part we introduce the structure of scan cell using a standard scan flip-flop from industrial design and discuss the existing tests for testing scan chains. Generally speaking, testing methods in order to enhance the testability of scan cells can be classified into two major types. One is to develop testing methods to generate tests other than the existing tests and the other is to change the design of the scan cell such that the internal faults are detected by the existing tests. The second part of this chapter reviews some test methods for scan cell internal faults. In the last part, we introduce some design for test methods to enhance the testability of scan cells. Finally, Section 2.4 summarizes this chapter.

2.1 The scan cell and existing tests

There are various flip-flop structures even for the same type of flip-flop. However, they operate in a similar manner and are obtained by cascading two latches each showing input logic values at one of the two clock phases (clock = 1 and clock = 0). One of a scan cell implementation is shown in Figure 2-1. It is a positive edge triggered Muxed input D flip-flop (MD flip-flop) whose transition table is given in Table 2-1. The circuit highlighted by the dashed rectangle is the multiplexer used for selecting between the functional data-in (D) and test scan-in (TI) inputs. The circuit between the nodes DP and MD is the master latch of the flip-flop and this is connected to the slave latch, the circuit between the node MD and the output (Q). When the test enable signal (TE) is set to 1 (0), TI (D) is selected. The value of TI (D) then propagates into the master latch when clock (CP) is low. Meanwhile, the nodes in the slave latch retain the values from the previous clock cycle. When CP turns to high, the signal stored in the master latch propagates into the slave latch and to the output of the scan cell.

The existing ATPG tools model scan flip-flops in scan chains as black boxes shown in Figure 2-2(a) and generate tests for faults at inputs and outputs of the scan flip-flops. The tests generated by ATPG targeting stuck-at and transition delay faults at data input (D) and output (Q) are called boundary SAF/TDF tests shown in Table 2-2 in this thesis. The test procedures are described as follows. The logic values required at the scan input (TI) of all scan cells are shifted into the scan chain with TE = 1 for n clock cycles (n is the number of scan cells in the scan chain). Then TE is toggled to 0 for one or more cycles so that the appropriate values will apply to the combinational logics, present at D inputs and finally propagate to the outputs of scan cells. The outputs of scan cells are shifted out for another n clock cycles to compare with the expected values thereafter. "Internal Faults On" command is an option often found in commercial ATPG tools. If the "Internal Faults On" command is used for the scan cell shown in Figure 2-2(a) the ATPG library model for the scan flip-flop used will be the one in Figure 2-2(b). However, this model still hides the transistor level implementation of the scan flip-flop. Thus, no additional test patterns are generated using "Internal Faults On" command. In addition, stuck-at faults (SAFs) and transition delay faults (TDFs) for both gate level and ATPG library models are equivalent and results in the same test patterns. Therefore, "Internal Faults On" option does not improve the coverage of internal faults of the scan cells.

In addition to the ATPG tests targeting D and Q, faults on TE, TI and CP and faults residing in the scan cell are assumed to be detected by what are called flush tests. The flush tests are used to ascertain the integrity of scan chains. Typically used flush tests are all zeros (00…0), all ones (11…1) and 0011 sequence repeated over the length of a scan chain (00110011…). The flush tests are scanned in and out of the scan chains with scan enable active (TE = 1) throughout the application of the flush tests. Figure 2-3 shows that the flush test 00110011… is applied to a scan chain with the length of n. The sequence 0011 is scanned in and out of the scan chain with test enable signal TE = 1 in Figure 2-3. The output is observed at the output Qn and compared with the expected

value. Obviously, faults in the circuit elements internal to the scan cells are not directly targeted during the flush tests. In the sequel, flush tests and ATPG boundary SAF/TDF tests are referred to as existing tests. Earlier works, [2.1-2.8], showed that existing tests miss many internal faults.

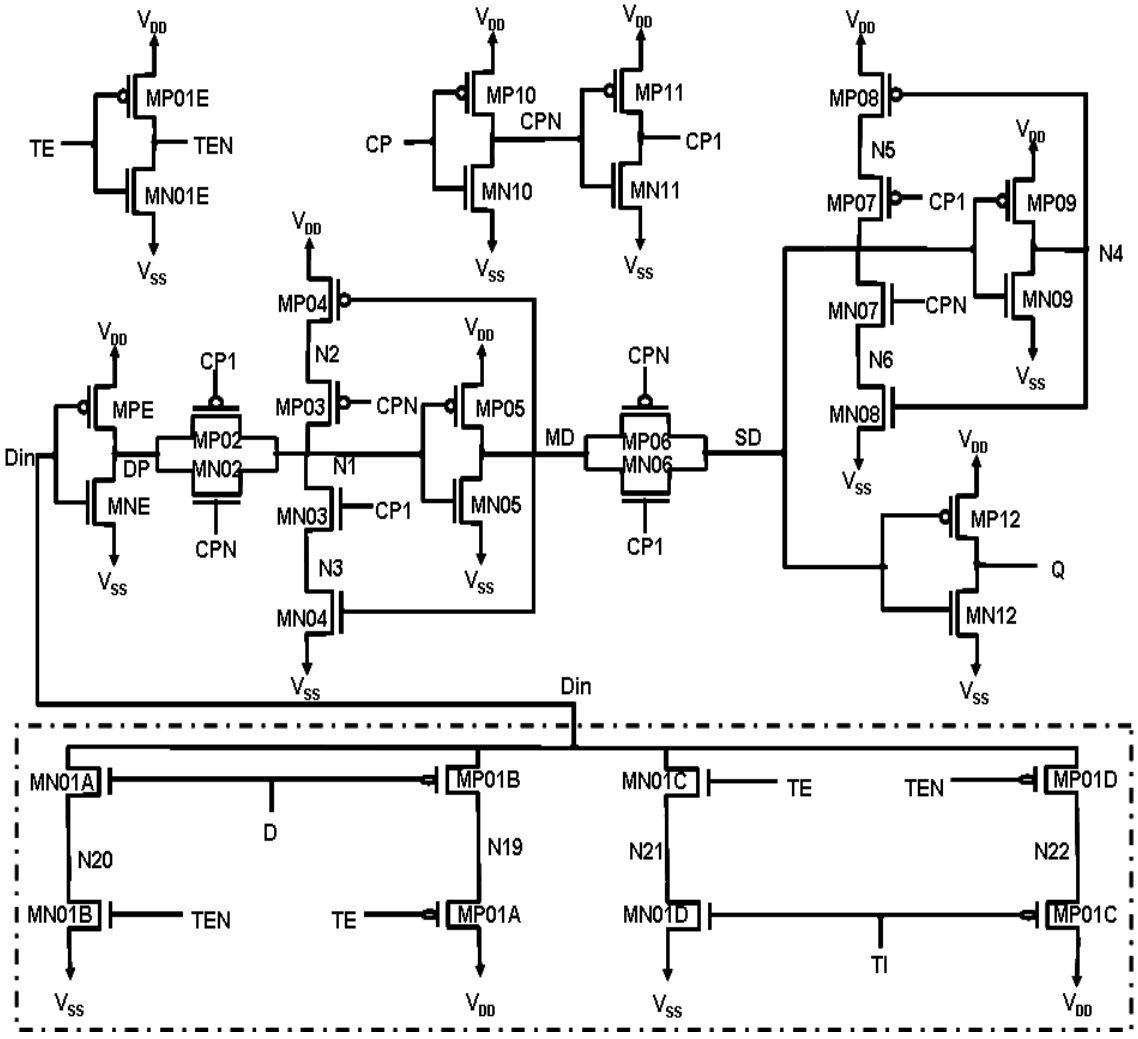


Figure 2-1: Scan flip-flop implementation

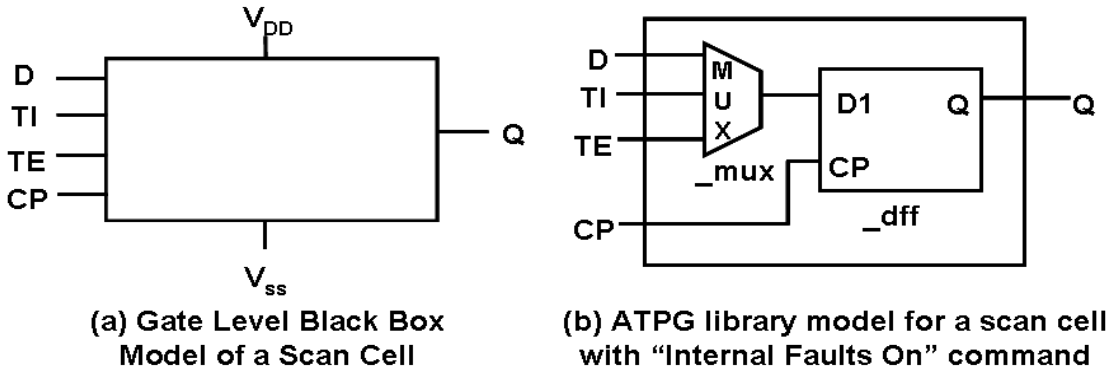


Figure 2-2: Gate level and ATPG library models for a scan cell

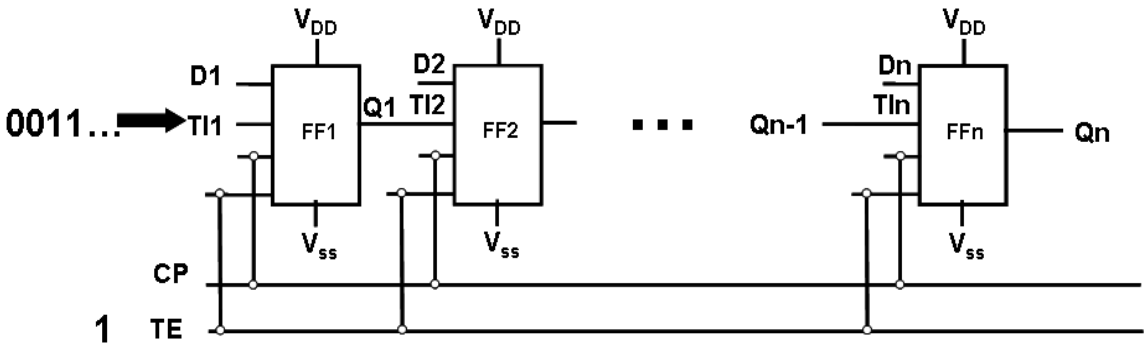


Figure 2-3: Application of flush test 00110011… to a scan chain

Table 2-1: Transition table of MD flip-flop

D	TI	TE	CP	Q
0	X	0	↑	0
1	X	0	↑	1
X	0	1	↑	0
X	1	1	↑	1

Table 2-2: Boundary SAF/TDF list and ATPG test patterns of scan flip-flop

Faults	Test Pattern
D stuck-at-0	D = 1, TE = 0, TI = X, Q = 1
D stuck-at-1	D = 0, TE = 0, TI = X, Q = 0
Q stuck-at-0	D = 1, TE = 0, TI = X, Q = 1
Q stuck-at-1	D = 0, TE = 0, TI = X, Q = 0
D slow-to-rise	D = 01, TE = 00, TI = XX, Q = 01
D slow-to-fall	D = 10, TE = 00, TI = XX, Q = 10
Q slow-to-rise	D = 01, TE = 00, TI = XX, Q = 01
Q slow-to-fall	D = 10, TE = 00, TI = XX, Q = 10

2.2 Test methods for testing of scan flip-flops

In this section, some previous works of test methodologies for detection of scan cell internal faults are reviewed. We first introduce a testing method relies on measuring the supply current in the quiescent state (when the circuit is not switching and inputs are held at static values). Then a method that models the scan flip-flop as a state machine and generates tests using the developed state tables is discussed.

2.2.1 Current testing (IDDQ testing)

In a fault-free quiescent CMOS digital circuit, there is no static current flowing from power supply to ground assuming leakage current is negligible. This is because under normal conditions, only gates of field effect transistors (FETs) are connected to the power supply (Vdd) or ground (Vss), and gates are highly insulated preventing DC current flow. Conducting paths from Vdd to Vss only exist during switching. Hence, the measured current in defect free circuit is small. However, many semiconductor manufacturing defects cause the current in the faulty circuit to increase by orders of

magnitude, which can be easily detected and differentiated from leakage currents. The testing method of measuring power supply current in the quiescent state of defective chips is called **current testing** or **IDDQ testing**. This method has the advantage of checking the tested circuit for many faults with one measurement. In addition, IDDQ testing is easier than voltage based methods in terms of generating the tests since IDDQ test vectors require only controllability and not observability. This is because the measurement is observed through shared power supply (Vdd).

For example, short which is usually modelled by bridging fault model is a common defect frequently presents in CMOS integrated circuits. To detect such fault, the two bridged nodes are set to opposite values. It has been shown when the bridge resistance increases above some resistance both faulty nodes will behave as in the fault-free circuit. However, the current flowing from one bridged node to the other node still presents even though it is weaker with increased bridge resistances. Therefore, in addition to the voltage based test methods IDDQ testing is one option to detect resistive bridging fault. [2.8] showed that IDDQ tests can detect many faults in scan flip-flops and latches not detected by the voltage-based tests.

As we mentioned earlier the capability of tester to sense the excess current is the key in this method. However, it may lead to higher start-up costs such as current sensor circuit design is required. In addition, as the new technologies continue to shrink the feature sizes of integrated circuits, the leakage current will not be neglected. Therefore, defining the “cut-off” current value to determine faulty IDDQ will be non-trivial.

2.2.2 Checking experiment method

The scan flip-flop has the structure with two latches cascaded where the operation involves the inputs changes during two clock phases (clock = 0 and clock = 1). In order to accomplish this in the testing, one can generate the test patterns that cover all possible inputs transitions from one clock phase to the other. In [2.4-2.8], Makar and McCluskey

proposed a checking sequence based tests set derivation procedures for testing faults internal to bistable elements (latches or flip-flops). The flip-flop is modeled as a state machine. It generates test for all transitions to the tested cell. In addition, both voltage-based method and IDDQ testing method are applied in the simulation results. **Checking experiment** is an input-output sequence that distinguishes a given state machine from all other state machines with the same inputs and outputs, and the same number of or fewer states [2.4].

The first step of the method is to create a primitive state table for the tested latch or flip-flop. The state table is developed based on the primary inputs and outputs. For the scan cell of Figure 2-1 which has 4 inputs and 1 output, there are 32 states. The primitive state table may be reduced from the operation limitations of inputs or operation assumptions. For example, it may assume that the value of scan-in (TI) can only change when CP = 1. Then the state transition from "CP = 0, TI = 0, TE = 1, D = 1" to "CP = 0, TI = 1, TE = 1, D = 1" is not allowed and can be deleted from the original state table. In the next step, a set of sub-sequences identify each state is derived. Finally, test patterns for all sub-sequences are defined.

The advantage of this method is that the test generation procedure does not require the internal implementation (circuit in transistor level) of the cell since the scan cell is modeled as a state machine. Hence, it is independent of scan flip-flop implementations. However, the checking sequence based method requires sequential ATPG procedures even for the circuit with full scan. In addition, it generates a large number of tests. The average size of the resulting tests, for ISCAS circuits, is 4.5 times the size of a single stuck-at test set which is a barrier to its use in practice. Since the checking sequence based method is a functional tests generation procedure, it needs to modify the existing ATPG which is expensive.

2.3 Design-for-test methods to enhance testability of scan flip-flops

In this section we give a brief review of design for test methods to enhance the testability of scan cells.

Many open defects affecting functional mode of operation of scan cells are hard to detect. Some of them in the transistors internal to scan cell may turn the scan flip-flop from a static state to a dynamic state. Consider the open fault denoted by an arrow in Figure 2-4. When CP = 1, logic value 1 enters the slave latch at node SD, N4 = 0 and output Q = 0 since transistors MP06 and MN06 are on. When CP switches to low, N5 is driven by Vdd since MP08 is on in the fault-free circuit. Hence N5 and Q hold logic value 1 and 0. In the faulty circuit, SD is floating when CP = 0 but still retains the logic value 1 from the last half cycle (when CP = 1) since SD discharge slowly (assume the open resistance between N5 and F is large enough such that the rate of charging SD is lower than the discharging rate). Thus, Q will remain at 0. Therefore, this fault is not detected. In functional mode of operation, if this flip-flop is not refreshed often enough, it may lose the stored information. This fault turns the scan cell into a dynamic flip-flop. If the clock is toggled often, the faulty scan cell functions properly, even though it is dynamic, since it is refreshed often. However, when clock is shut-off during clock gating, SD is floating. If SD was set to 1 prior to this then the fault will appear when we get out from the clock gating phase. This is a problem if state retention is required. Frequency scaling is another scenario when such faults could manifest themselves due to the current leakage. Such problem is identified in [2.2] and a design of D-latch which can be used to compose flip-flop is proposed. A clocked D-latch shown in Figure 2-5(a) is studied in [2.2]. PFETs P3 and P4 and NFETs N3 and N4 are not detected because of the reason described above. Those faults may be detected by applying tests at very slow speed to let the voltage at node Q1 discharge/charge to the faulty value. However, the time required to reduce the voltage at node Q1 in Figure 2-5(a) depends on the capacitance at this node

and leakage current. In addition, this method increases the testing time which may not be cost-effective. In order to detect such faults, the data and the clock signals are required to be independently controllable. The D-latch shown in Figure 2-5(a) is augmented with an additional controllable input, C, as shown in Figure 2-5(b). During normal operation C is set to 1 and during testing operation C can be changed irrespective of the state of the clock. For example, to detect open fault in P3, the test sequence, T1 (CL = 1, D = 0, C = 1, Q1 = 0), T2 (CL = 0, D = 1, C = 1, Q1 = 0), T3 (CL = 0, D = 1, C = 0, Q1 = 0), T4 (CL = 1, D = 1, C = 0, Q1 = 0), T5 (CL = 0, D = X, C = 0, Q1 = 0) and T6 (CL = 0, D = X, C = 1, Q1 = 0), is applied. However, this design introduces one primary input and four transistors. Hence, it increases the size of the scan cell which is not practical.

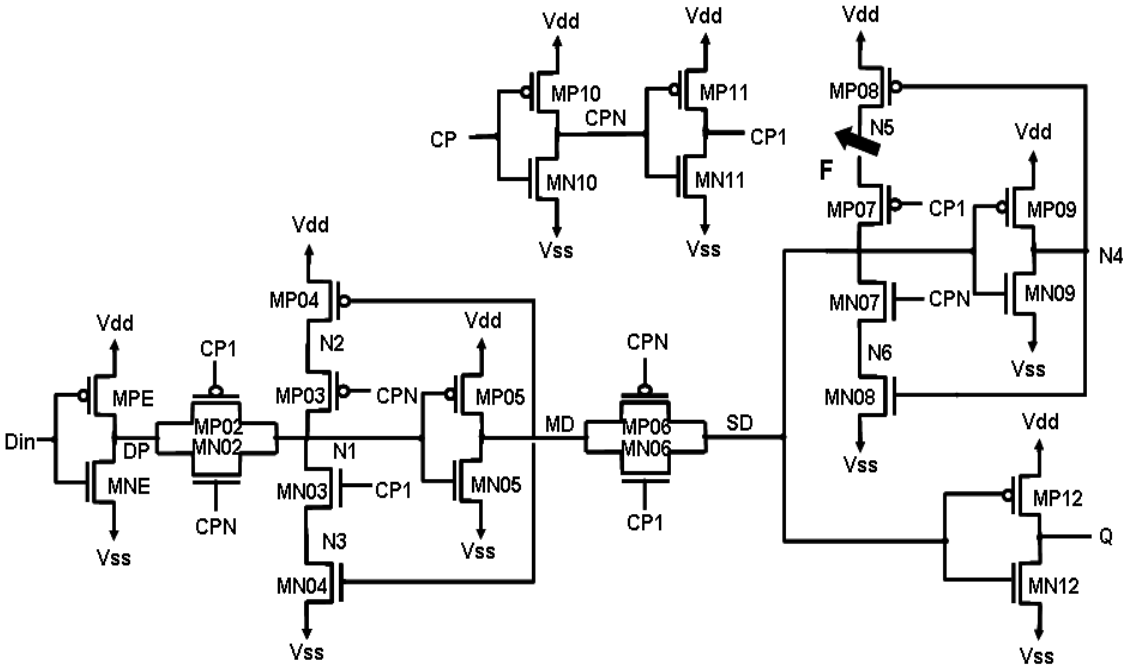


Figure 2-4: Open fault turns scan cell into dynamic state

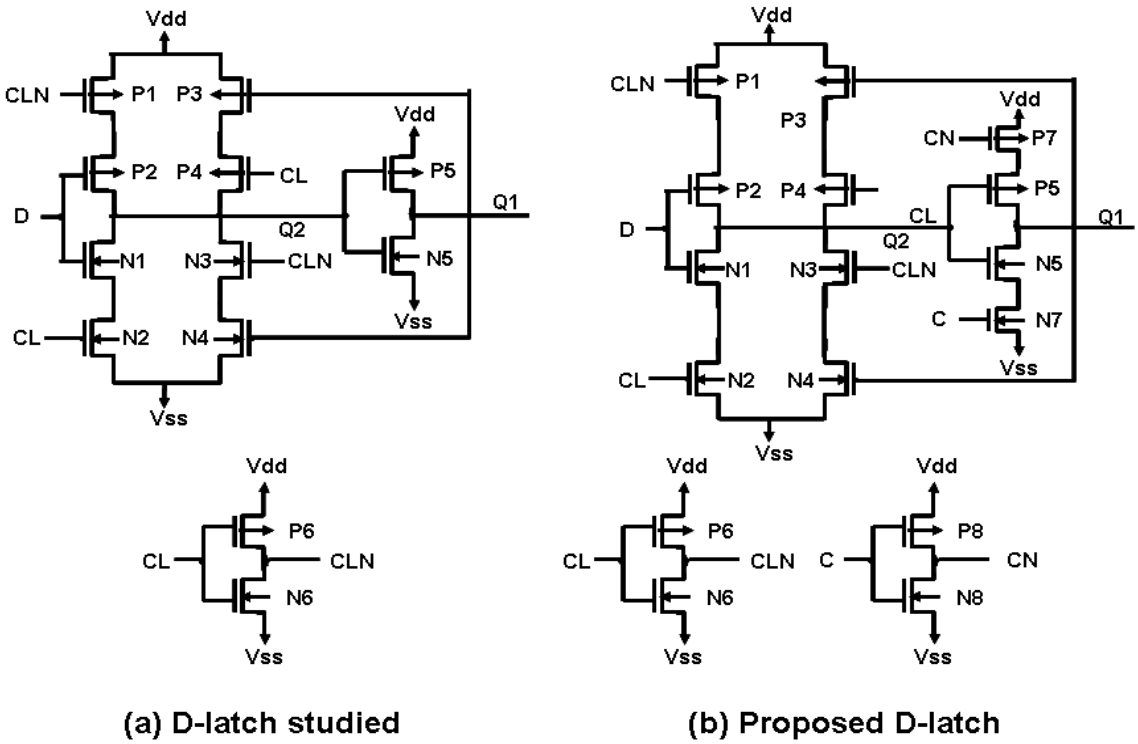


Figure 2-5: D-latch used and proposed in [2.2]

Obviously, stuck-open faults in the serial path are easily detectable, because the output of every gate on the serial path is uniquely set by tests. On the other hand, open faults in the branches in the parallel path are much harder to detect and they represent the main problem. For example, the master latch and latch stage in Figure 2-1 are shown in Figure 2-6. Consider the open faults denoted by arrows in Figure 2-6. They are not detected since one of the transistors in the transmission gate is open will not block the signal propagation from multiplexer to the master latch. To solve this problem, one can change the design shown in Figure 2-7. It is a scan cell implementation where four clocked inverters composed by MP02 and MPX1, MN02 and MNX1, MP06 and MPX2, and MN06 and MNX2 are used instead of the transmission gate between the master latch

and slave latch. By replacing the transmission gates in Figure 2-6 with the clocked inverters as shown in Figure 2-7, those untestable stuck-open faults do not exist. However, this implementation may degrade the scan cell performance. The transmission speeds from multiplexer (DP) to master latch (N1) and master latch (MD) to slave latch (SD) is reduced since two transistors in parallel is replaced by a single transistor between them which increases the resistance.

The problem of undetected opens in parallel branches can also be solved by removing the redundant part of circuit. [2.9] proposed to change the design of a scan cell at transistor level without changing the logic behavior of the circuit. This can be done by identifying the partial redundancies, i.e. those circuit elements that do not cause any change in logic behavior, but cause other behavior changes, e.g., change in timing (signal transition speed). For example, one of the transistors (e.g. MN02) in transmission gate in Figure 2-6 can be removed.

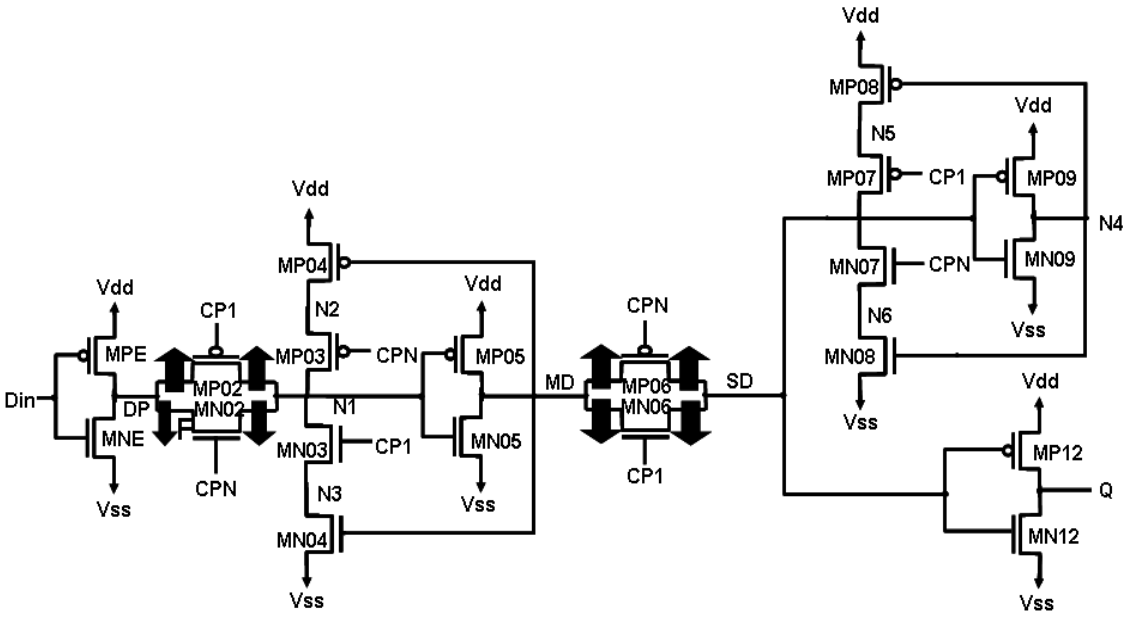


Figure 2-6: Undetected stuck-open faults (SOPs) in Figure 2-1

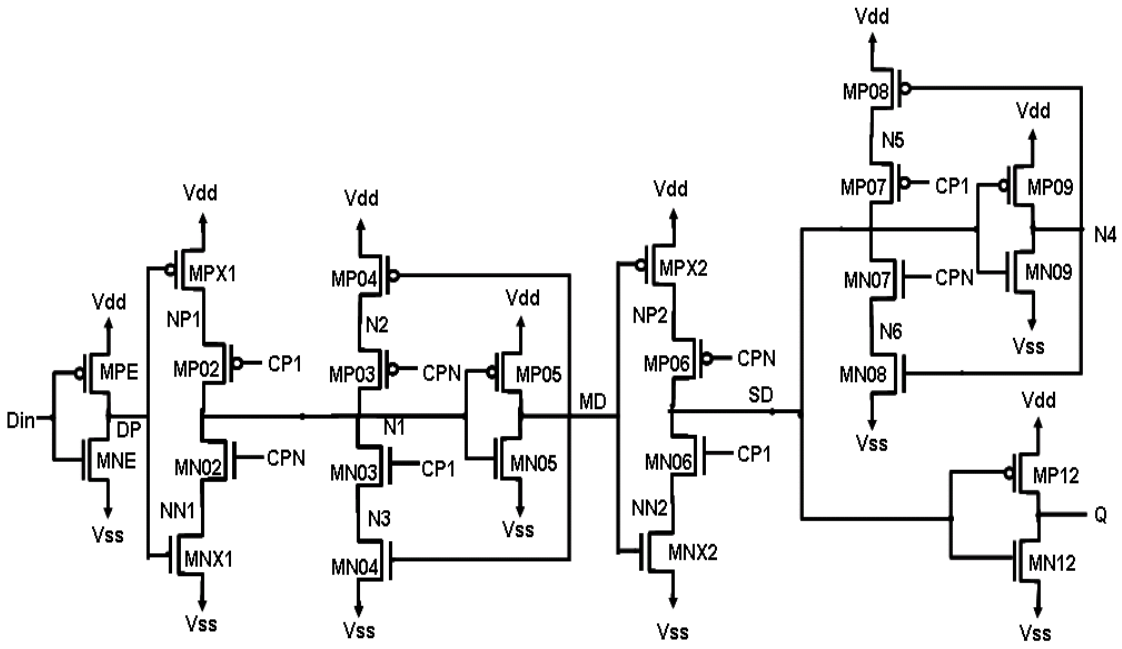


Figure 2-7: Clocked inverters used

2.4 Summary and remarks

This chapter shows that ATPG patterns only target inputs and outputs of scan cells and do not give high coverages of the defects internal to the scan cells. Those faults not detected may lead to functional failures or pose reliability issues. It had been shown that IDDQ tests were effective to detect a large portion of scan cell internal faults. Especially for large resistance bridging faults, the faults may not be detected by logic testing because the two bridged nodes may take the fault-free logical values. However, as feature size of VLSI decreases (45nm is coming up), the faulty quiescent current is too small compared to the total chip nominal current. Determining the current limit to differentiate faulty and fault-free circuit is crucial and difficult since it is a dynamic value depending on bridge resistance, power supply voltages and transistor threshold voltages, etc. Thus, the IDDQ only detectable faults will become an important contributor to test escapes.

In addition to the fault coverage, testing cost in terms of test pattern size is another major concern to detect scan cell internal faults. Some methods such as checking sequence based tests reviewed in this chapter are not practical due to the large size of tests and difficulty to generate the tests.

Changing the scan flip-flop design or layout may be an alternative method to improve the scan cell testability. However, the considerable overhead area added and cell performance degradations introduced by the new designs are critical issues need to be carefully considered.

CHAPTER III ON DETECTABILITY OF SCAN CELL INTERNAL FAULTS USING STUCK-AT AND STUCK-ON FAULT MODELS

Stuck-at fault model has been extensively used in the industry to mimic defects at lines and nodes in circuits. Defects in transistors are usually modeled by stuck-on fault model. In this chapter, we present the first step in developing an alternative test methodology for scan cell internal faults by using stuck-at and stuck-on fault models. A new flush test is proposed to improve the stuck-at and stuck-on fault coverage. Other conventional methods, IDDQ testing and low power supply testing, are also investigated to cover the identified coverage gaps. Experimental results on a standard scan cell used in a 90 nanometer industrial design are included.

3.1 Introduction

As shown in Chapter I, there are a large number of faults residing in scan cells. Thus, it is important to determine the coverage of faults internal to scan cells and if necessary investigate cost effective methods to augment tests generated by standard automatic test pattern generation (ATPG) procedures to improve coverage of scan cell internal faults.

In this chapter we report the results of a case study on an industrial design. We report fault coverage using standard test patterns and flush tests. The study exposes test coverage holes that need to be addressed. We also propose a new flush test called half-speed flush test that closes some of the coverage holes. In order to achieve the defect coverage or lowest Defects Per Million tested devices (DPMs), the defect behaviors need to be described as accurately as possible. Such defect behaviors are described by many fault models. In this chapter, we focus on detection of stuck-at faults (SAFs) and stuck-on faults (SONs) internal to scan cells.

It has been noted that many faults internal to latches and flip-flops may not be detected [3.3-3.11] by standard scan based tests. In Chapter II, we reviewed a checking

sequences based test method and showed that it is not practical due to the large size of tests generated and difficulty to generate the tests.

Noting that some of the transistor stuck-on faults cannot be detected by voltage based tests, a testable design of latches was proposed by Aissi and Olaniyan [3.11]. Use of this design increases the area of scan cells and requires two additional primary inputs to control internal nodes of scan.

The goal of our work is to investigate the use of standard scan cells and existing methods of generation and application of scan based tests to detect scan cell internal faults. In this chapter we present results of the first step in this direction. The main contributions of the work presented are:

(1) Defining the notion of half-speed flush test and demonstrating that half-speed flush tests increase coverage of internal faults in scan cells.

(2) Demonstrating that existing test generation and test application methods together with the half-speed flush test cover cell internal faults to similar degree as the checking sequence based tests.

(3) Showing that IDDQ testing of 90nm and beyond designs may not be feasible for a significant portion of the faults leaves coverage holes which, in addition to the issue of quality of shipped products, could result in a serious reliability risk.

We quantify the above using a 90nm commercial product described in Table 1-1 which consists of approximately 4.3 million cells and 54 million transistors.

The remainder of the chapter is organized as follows. In Section 3.2 we briefly discuss related earlier works on the detection of scan cell internal SAFs and SONs [3.5-3.10]. The stuck-at and stuck-on fault models and some test methods for such faults are also reviewed. In sections 3.3 and 3.4 we discuss the half-speed flush test we defined and the probabilistically detected faults. In Section 3.5, we present the HSPICE simulation

results on scan cell internal faults and discuss the conclusions from the simulation results. Finally, Section 3.6 concludes this chapter.

3.2 Preliminaries

In this section we briefly review the stuck-at and stuck-on fault models. The conventional test methods targeting these faults are also presented. In addition, we will discuss some related earlier works on the detection of faults in scan cells applying these fault models.

3.2.1 Stuck-at and stuck-on fault models

Fault models are abstraction of defect behaviors and test patterns are generated by targeting certain fault models which describe the defects as accurate as possible. The investigations in this chapter focus on scan cell internal faults using stuck-at and stuck-on fault models.

Stuck-at fault model is the most widely used fault model in which represents a single line being permanently stuck at a logic value (1 or 0) which is caused by unwanted shorts between the line and power supply (Vdd) or ground (Vss). Figure 3-1(a) shows that the gate (node a) of a PMOS stuck-at 0 and the source (node c) stuck-at 1 faults. This fault model is independent of the technology, as the concept of a wire being stuck at a logic value can be applied to any structural model. It was also been found that the tests based on this model detect many unmolded defects.

In addition, the stuck-at fault model can be used to model other types of defects. For example, NMOS transistor **stuck-on fault** where the faulty transistor is permanently turned on can be modeled by the gate of the NMOS transistor stuck-at 1 shown in Figure 3-1(b). Note that when counting nodes for considering scan cell internal faults, stuck-at fault model may not consider fan-out branches. For example, although node N4 has two branches in Figure 2-1, only two stuck-at faults (N4 stuck-at 1 and N4 stuck-at 0) are

considered. N4 stuck-at-0 makes transistors MP08 stuck-on and MN08 stuck-off. This is different from the gates of MP08 and MN08 stuck-at-0 independently. The stuck-on fault can be caused by intra-gate shorts (the shorts between the drain and the source of the faulty transistor) and gate to power supply shorts.

The stuck-at fault model has been extensively used in industry for decades. For the detection of single stuck-at fault, we must activate the fault by setting the logic value opposite to the faulty value at the faulty site. For example, to activate the fault a/0 in Figure 3-1(a) the node a is set to 1 which involves the line justification. The line-justification problem deals with finding an assignment of primary input values that results in a desire value setting on a specified line in a circuit. The controllability is used to measure the difficulty of setting a line to a value. In order for the detection of a fault, fault propagation is required where primary inputs are set to appropriate values such that the fault is able to propagate to at least one of the primary outputs (i.e., one or more primary outputs present the faulty value due to the fault). The ability of fault propagation is measured by the observability which indicates the relative difficulty of propagating an error from a line to a primary output.

The detection of defects applying stuck-on fault model is similar to the detection of stuck-at fault. Instead of activating the fault by setting fault-free value at the faulty site, the gate of the faulty transistor is set to 0 for NMOS and 1 for PMOS which attempts to turn off the faulty transistors.

3.2.2 Previous related work

A checking sequence based tests [3.6-3.9], discussed in Chapter II, have the advantage of independent of scan cell implementation. A sequential ATPG is required

even for full-scan circuits. The complexity of the sequential test generation process restricts its use to small circuits.

Applying checking sequences based tests to muxed-input scan cell shown in Figure 3-2, the following fault coverage was obtained in [3.8]: 31 out of a total of 32 (96.9%) SAFs and 18 out of a total of 26 (69.2%) stuck-on faults (SONs) are detected without using IDDQ. With IDDQ testing, one more SAF and 5 additional SONs are detected, thus making SAF coverage 100% and SON coverage 88.5%.

3.3 Half-speed flush test

Scan input TI (cf. Figure 3-3) of a single flip-flop in a scan chain gets its value from the output of the previous flip-flop which changes value at shift clock rising edge. There is a path delay between the two stages. Thus TI can change value either within the half cycle where CP = 1 if the path delay is less than half shift clock period or the half cycle where CP = 0 when the path delay is greater than half of the shift clock period. In the fault-free circuit a new value can propagate to the output of a flip-flop only when it arrives within CP = 0. However, we found that detection of some cell internal faults require that scan input TI change when CP = 1. To detect such faults we define a new type of test called *half-speed flush test*. For example, Figure 3-3 shows line CP1 stuck-at-0 (highlighted by arrows on the fan-out branches of CP1). This fault makes transistors MP02 and MP07 to be always on and transistors MN03 and MN06 to be always off. We refer to Figure 3-3 and Figure 3-4 in the following discussion of this fault.

To detect CP1 stuck-at-0 fault, we can first set Q to 0 in clock cycle i by setting TI to 0 when CP = 0. After that we set TI to 1 in clock cycle i+1 when CP = 1. In the fault-free circuit, this change of TI in shift clock cycle i+1 will not propagate to Q, since MP02 and MN02 are turned off when CP = 1. However, in the faulty circuit, this change in TI, during clock cycle i+1, will propagate to Q in clock cycle i+1, since MP02 is on due to the fault and MP06 is on since CP = 1. This is shown in Figure 3-4(a), where solid

lines are signals from fault-free circuit and dashed lines show faulty waveforms. By a similar argument, as shown in Figure 3-4(b), we note that if instead of changing TI when CP = 1 in clock cycle i+1 we change TI when CP = 0, then the fault will not be detected.

Detection of faults by changing TI when CP = 1 poses a problem. During test application we will not be able to change TI directly, but indirectly through the output of the previous flip-flop in the scan chain. We next discuss a method to accomplish this.

In Figure 3-5 three MD flip-flops are cascaded to form a segment of a scan chain. Assume the fault discussed above occurs in the second scan flip-flop of Figure 3-5. TI1 gets its value from the previous scan flip-flop output (Q0) in the scan chain. There is a path delay between Q0 and TI1. Assume that the shift mode of the scan chain has been closed during timing closure for f mega hertz (i.e. the maximum delay between Q0 and TI1 is T = 1/f). Then the propagation delay (d) from Q0 to TI1 lies between 0 and T. Let us assume that the shift clock period is S. Q0 = 00110 (a segment of flush test), is produced at the shift clock rising edge. Therefore, TI1 changes within CP = 1 if d is smaller than S/2. As discussed previously, if the path delay results in TI1 transition within CP = 1, then this fault can be detected by the flush test. Whereas the fault cannot be detected if d is greater than S/2, causing TI1 to change within CP = 0. Figure 3-6 shows the waveforms when the shift cycle time S = T. The path delay between Q0 and TI1 is greater than S/2 causing TI1 to transition within CP = 0. By observing outputs of scan flip-flops Q1 and Q2, as discussed above, the fault is not detected. But, we can expand the clock until TI1 transitions within the half cycle with CP = 1. This can be accomplished by slowing down the scan shift speed during the application of the flush test 00110011…. Figure 3-7 shows that the fault is detected by applying the flush test with scan shift cycle period S = 2T. The dashed lines show faulty waveforms and the solid lines are fault-free waveforms. Starting from rising edge R3, faulty value (00110/11100) of Q2 is generated. This flush test with shift clock period S no less than

2T detects the fault with path delay both greater and smaller than T/2. S = 2T is preferred in order to maximize the flush test shifting speed.

This motivated our definition of half-speed flush test. Assume that we have timing closure of scan chain at frequency f, then the shift speed for half-speed flush test will be at frequency f/2 or less. For example, if timing is closed at 10 mega Hertz (200 MHz) half-speed flush test runs at 5 mega Hertz (100 MHz) or less. Note that we only slow down the flush test 00110011....

In [3.8], the authors discussed slow speed application of the checking sequences. The motivation for that was to detect additional stuck-open faults (SOPs). In [3.8], the above mechanism of detecting such scan cell internal faults using flush tests was not considered. Furthermore, the frequency for the test we are proposing is related to the timing closure frequency of the scan chains of the design.

3.4 Probabilistically detected faults

Probabilistically detected faults are faults that are not proved to be detected but have a high probability of detection. Consider node N19 stuck-at-1 highlighted by an arrow in Error! Reference source not found.Error! Reference source not found.. The detection condition for this fault is D = 0, TE = 1, TI = 1, Q = 1. Since TE = 1, it cannot be detected by a scan cell boundary SAF test. Assume that initially the scan chain has random bits and the length of the scan chain is L. Consider the case when the flush test 00110011… is applied to the scan chain. Data input D, which is driven by the combinational logic, can be either 0 or 1. If we assume that D = 0 or D = 1 with equal probability, then the probability that N19 stuck-at-1 is not detected by the flush test is $(4/5)^L$. When the flush test of all ones is applied, the probability that the fault is not detected, under the same assumptions on D, is $(1/2)^L$. In typical industrial designs L can be about 1000. Thus the fault can be assumed to have been detected by the flush test. In this work we say that the fault is assumed probabilistically detected. We perform such

probability analyses to identify faults which can be classified as probabilistically detected.

3.5 Experimental Results

In our HSPICE based simulation, we used the segment of a scan chain shown in Figure 3-5. A target fault is injected into the second scan cell by modifying its circuit description. To simulate SAFs, we connect the faulty node to Vdd (stuck-at-1) or to Vss (stuck-at-0). A SON is modeled by connecting the gate of a faulty NMOS transistor to Vdd and the gate of a faulty PMOS transistor to Vss. There are a total of 44 SAFs and 34 SONs. Table 3-1 summarizes the simulation results. The number of faults detected by normal speed flush test, with the corresponding percentage is shown in column 2. The additional number of faults detected by half-speed flush test is shown in column 3. It is important to note that even though we do not explicitly show this in Table 3-1 all faults detected by the flush test 00110011... applied at normal shift frequency are also detected by the half-speed flush test. Thus one only needs to apply the flush test at half-speed to detect all the faults reported detected by the flush test. Column 4 shows the number of faults not detected by flush test and detected by scan cell boundary SAF tests. Fifth column shows the number of probabilistically detected faults. The last column gives the total number of undetected and IDDQ only detectable faults. The second row is the results for SAFs. Results for SONs are presented in the row 3, respectively. Next we discuss each of these rows in details.

From Table 3-1 we observe that 34 (77.3%) out of 44 SAFs are detected by flush test, and another 1 (2.3%) fault is detected only by the half-speed flush test. Third column shows that boundary SAF tests detect 5 (11.3%) additional SAFs that are not detected by the two flush tests. Four faults (9.1%), N19 stuck-at-1, N20 stuck-at-1, TE stuck-at-1and TE stuck-at-0, are probabilistically detected. We compare this result with D flip-flop results from [3.8]. Out of a total of 24 SAFs one fault was not detected by the checking

experiments and required IDDQ testing. In our case, all SAFs are detected without IDDQ, assuming that the probabilistically detected faults are indeed detected. Given the uncertainty of using IDDQ for future technologies, removal of this dependency on IDDQ tests is a significant step forward. Half-speed flush test also increases SAF coverage by 2.3% for a cell and by 1.03% for the full-chip using the data for the industrial design in Table 1-1. Given that today's designs attempt to achieve over 99% coverage this increase is quite significant.

From Table 3-1 we note that the flush test detects 11 (32.4%) and another 3 (8.8%) SONs are covered by half-speed flush test. Scan cell boundary SAF tests detect 1 (2.9%) additional fault. The faults MN01B, MP01A and MN01E stuck-on faults are probabilistically detected. The remaining 16 (47.1%) SONs are not detected by Boolean tests. However, 12 (35.3%) of these faults can be detected by IDDQ testing if such measurements are feasible. Comparing with the results from [3.8], 4 out of a total 20 SONs in the D flip-flop considered in [3.8] were not detected by the checking experiment based tests. If we restrict ourselves to the two latches of the MD flip-flop used in our design, we get the same coverage as [3.8] but without using the long checking sequences. Once again note the importance of the half-speed flush test. It added about 8.8% SON coverage per cell.

3.5.1 Coverage gaps identified

The last column of Table 3-1 shows that fault coverage gaps still exist. Many of them are IDDQ detectable only. By simulating a scan cell using HSPICE we determined that for all the IDDQ only detectable faults, the IDDQ through the transistor affected by a fault is within 1μA when the fault is not present and the IDDQ is in the range of 47.71μA to 365μA in the presence of the fault. For the 90nm product under study the faulty IDDQ is less than 0.04% of the nominal total chip IDDQ. Hence, we believe that full chip IDDQ based measurements will not detect such defects.

We note that many of the defects that require IDDQ testing will be activated during the functional mode of operation. Consider the example in Figure 3-8 where MN01C SON is highlighted by a dashed circle. For MN01C SON the test condition is D = 0, TE = 0, TI = 1, Q = 0. A Vdd to Vss path is formed in the multiplexer. IDDQ for fault-free circuit remains as low as 1μA, whereas it is 47.8μA for this faulty circuit. Note that this condition will be satisfied during the functional mode of operation. Whenever this condition is satisfied MP01A and MP01B sink about 47 times more current. This current surge is a major reliability issue for these transistors.

Using the data in Table 1-1, we estimate that the percentage of IDDQ only detectable SONs is approximately 35.3% of the transistors in the logic. This poses a potential reliability risk if not addressed.

An alternative to detecting such defects could be low voltage testing. For the fault in Figure 3-8, we performed a simulation and the results are given in Table 3-2. In order to detect the fault, the supply voltage was progressively lowered. Note that only when the supply voltage was reduced by more than 50% the output showed a faulty value. However, lowering voltage by more than 50%, we believe, is not feasible and therefore low voltage testing cannot be used. An alternative test for such defects is thus required.

We performed probabilistic analysis using simple assumptions and found that 9.1% and 8.8% of SAF and SON of the cell faults are probabilistically detected shown in column 5 in Table 3-1. Translated using the data from Table 1-1, this implies full-chip coverage of 4.08% SAFs and 3.83% of SONs. Considering desired SAF target coverage in the high nineties this is very large. It is therefore important to determine what percentage of the probabilistically detected faults is actually detected. Additional tests may be required to cover any coverage gaps found.

3.6 Conclusions

The detection of scan flip-flop internal faults is important as it may result in functional failure. Nearly 50% of the SAFs reside in the scan chains and are currently not directly targeted for test generation. The earlier proposed method of using checking experiment [3.8] to detect these faults is not practical because of its large size and the difficulty of deriving the tests. An analysis of SAFs and SONs in a MD flip-flop using flush tests and boundary stuck-at tests was presented in this chapter. We proposed a new flush test called half-speed flush test and showed that it improves fault coverage by a couple of percentage. We also identified that a large proportion of faults are probabilistically detected. It is important to verify with product data if these faults are actually detected by the ATPG and flush tests. We showed that there is also a large class of IDDQ only detectable faults that poses a serious reliability risk. Given these gaps, we believe, alternative tests to detect these faults are required.

Table 3-1: HSPICE simulation summary

	Normal Flush Test	Half-speed Flush Test	Boundary SAF Tests	Probabilistically Detected	IDDQ /Undetected
SAF	34 77.3%	1 2.3%	5 11.3%	4 9.1%	0 0%
SON	11 32.4%	3 8.8%	1 2.9%	3 8.8%	16 47.1%

Table 3-2: Low Vdd testing of MN01C SON fault at 25°C with test: D = 0, TE = 0, TI = 1, Q = 0

Vdd	1V	0.8V	0.7V	0.42V
Q	0	0	0	0.42

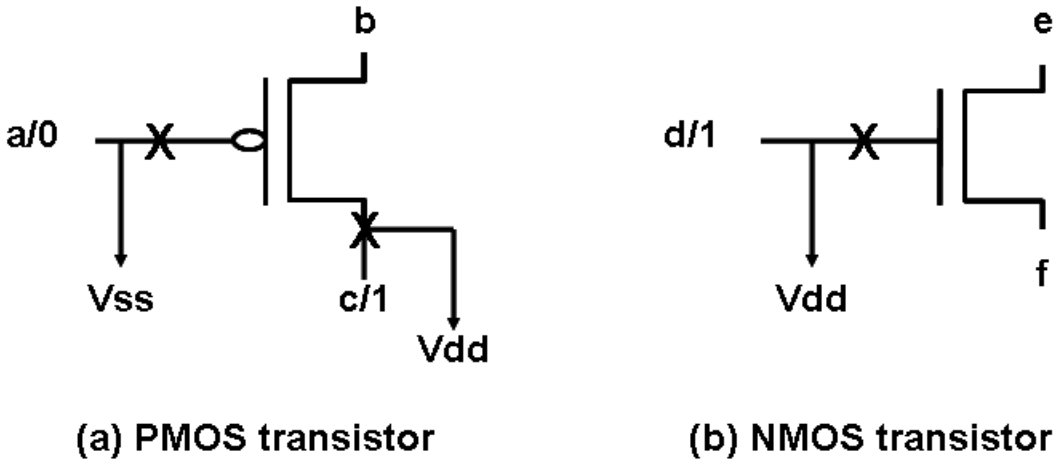


Figure 3-1: Stuck-at fault model

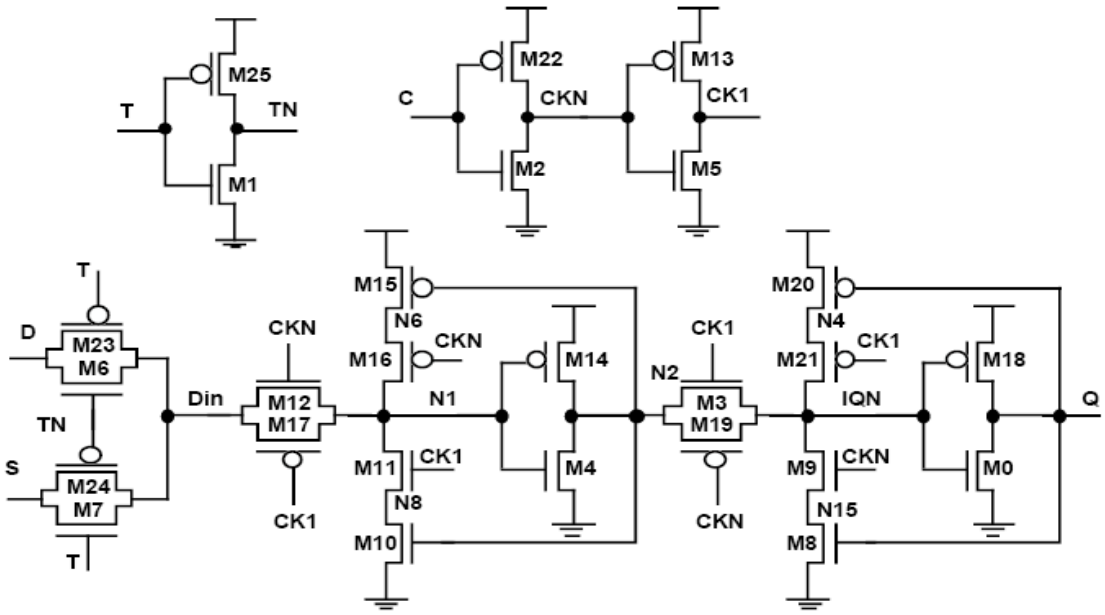


Figure 3-2: Scan cell used in [3.8]

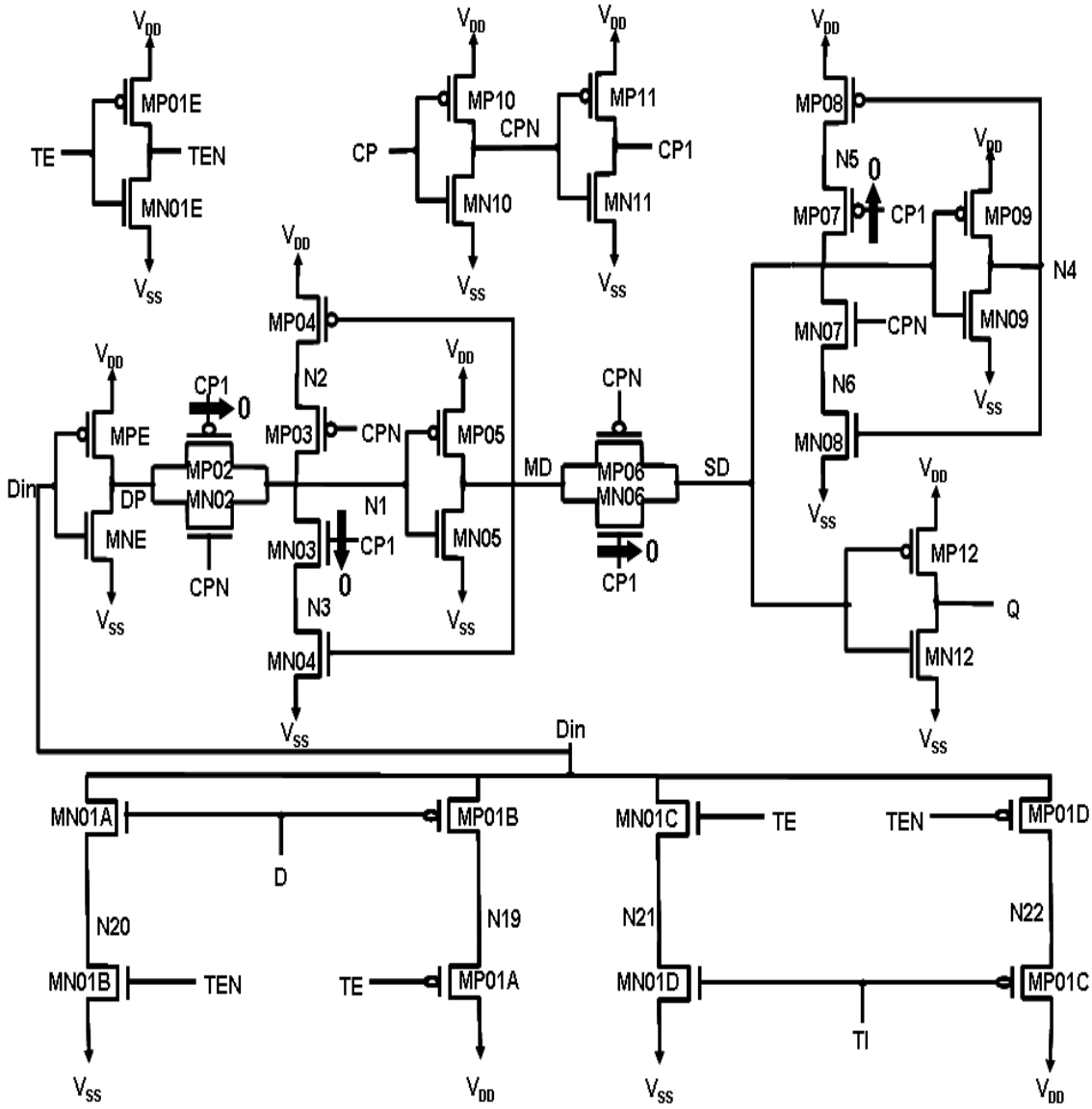


Figure 3-3: Fault CP1 stuck-at-0

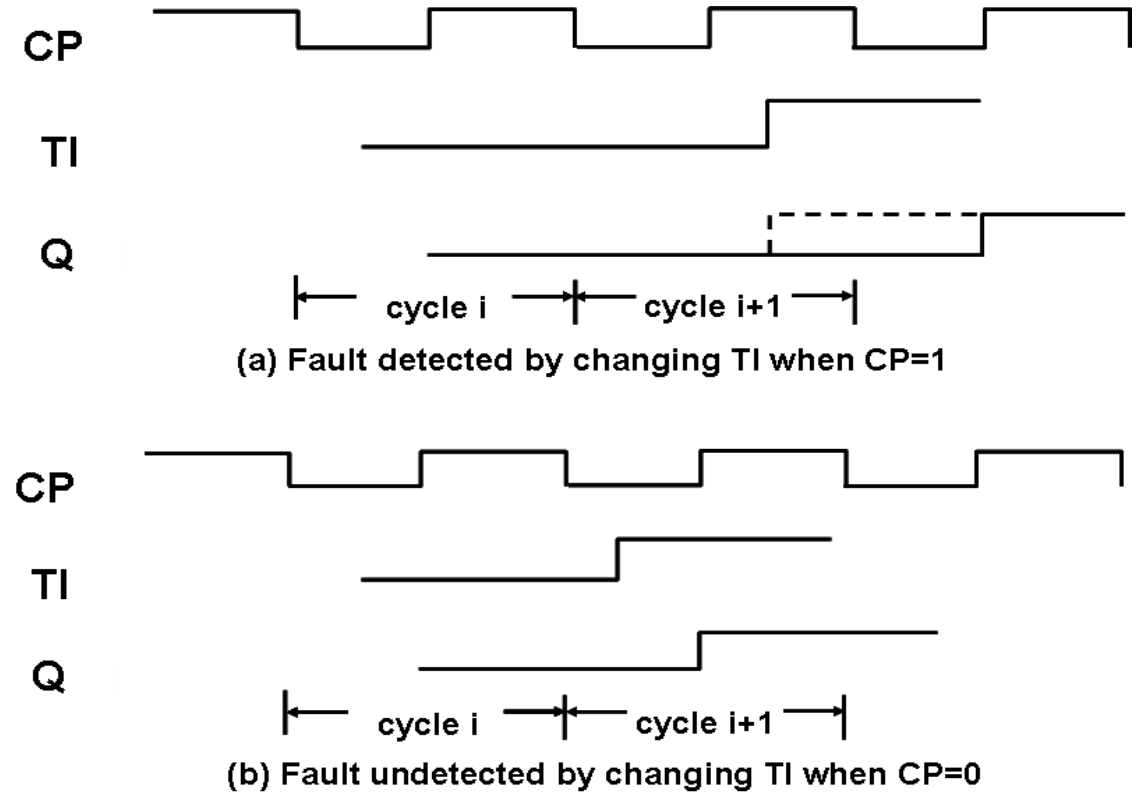


Figure 3-4: Detection of the fault CP1 stuck-at-0

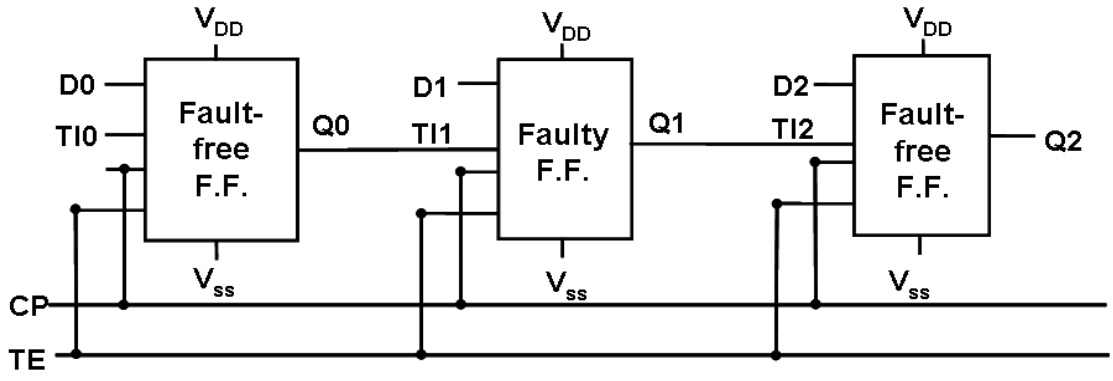


Figure 3-5: Logic diagram of a scan chain with length 3

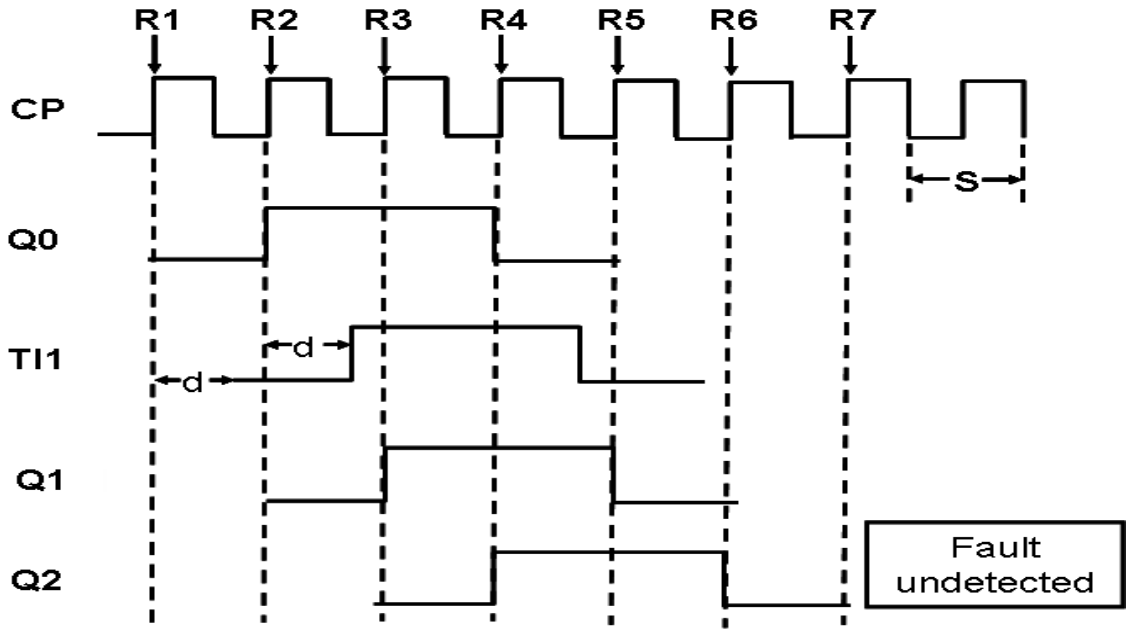


Figure 3-6: Detection of CP1 stuck-at-0 with S = T

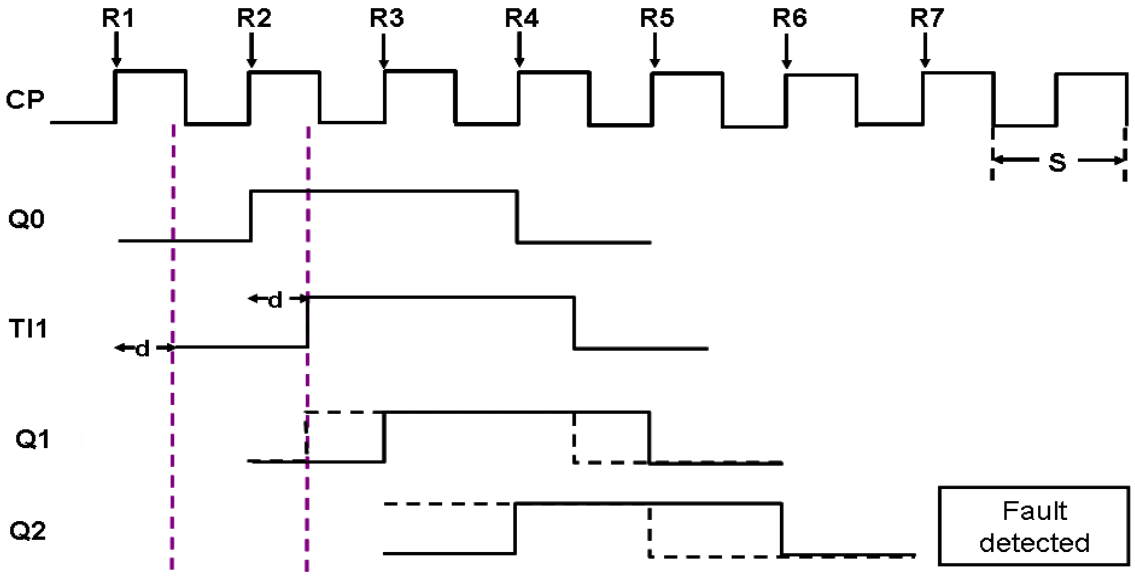


Figure 3-7: Detection of CP1 stuck-at-0 with S = 2T

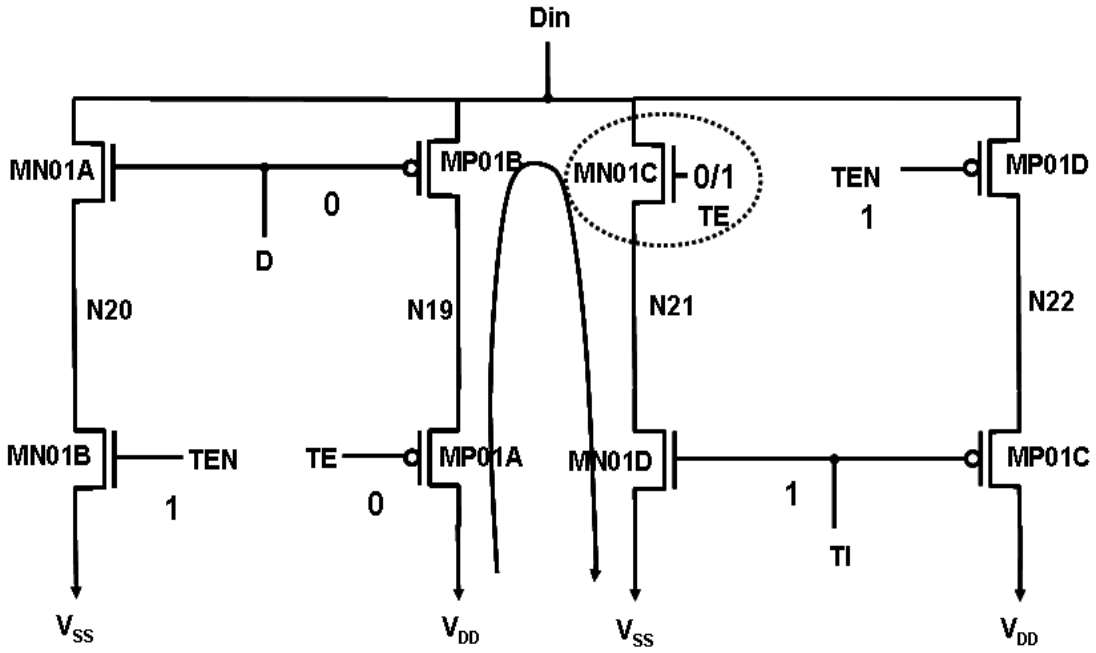


Figure 3-8: IDDQ testing of MN01C SON

CHAPTER IV ANALYSIS OF DETECTABILITY OF INTERNAL BRIDGING FAULTS IN SCAN CELL

In this chapter, we report a comprehensive analysis of detection of a set of scan cell internal bridging faults extracted from layout. Both zero-resistance and nonzero-resistance bridging fault models are considered. Some observations on detection of internal bridging faults are presented. We classify the undetectable faults based on the reasons for their undetectability. A low power supply voltage based test method and IDDQ testing are also examined for resistive bridging fault detection. Experimental results on a scan cell used in a 90 nanometer industrial design are included.

4.1 Introduction

In Chapter III, we studied the detectability of SAFs and SONs internal to the scan cells. We showed that the cell boundary tests and a new flush test applied at a frequency related to the timing closure of the scan chain achieve fault coverages similar to those achieved by checking sequence based tests in [4.4-4.7].

Experimental analysis and studies [4.12-4.17] based on Inductive Fault Analysis (IFA) have shown that a short between physically adjacent lines, which is called a bridging fault, is a frequent defect mechanism in CMOS IC's. Manufacturing tests based on the stuck-at fault model are becoming less effective in detecting defects which are typically resistive opens and shorts.

A vast volume of work has been done previously to model [4.19-4.24] and detect [4.25-4.28] bridging faults. A few works considered bridges internal to scan cells [4.29-4.31]. IDDQ testability of bridging faults in flip-flops was analyzed in [4.29-4.31]. A modified flip-flop introduced to improve the testability of internal bridging faults [4.31] increases the size of the scan cells quite significantly and hence may not be practical.

In this chapter, we consider bridging faults internal to scan cells. We consider the case where the resistance of the bridge is negligible as well as resistive bridging faults

with non-negligible resistances. We investigate the detectability of a set of realistic bridging faults extracted from the layout of a scan cell implementation. HSPICE simulation of scan cell internal bridges is used in a 90 nanometer commercial product. In this product, the scan cells contain approximately 45% of the transistors in the design. The tests we used are flush tests and ATPG generated tests. From the analysis, we show that both single pattern and two-pattern tests are required to cover all the detectable bridging faults, even for the non-resistive bridging faults. Earlier proposed IDDQ based tests and low power supply voltage tests are also investigated to cover bridging faults not covered by the normally used flush tests and ATPG boundary SAF/TDF tests. The main contributions of this work are the following:

(1) Demonstrating for the first time that detection of some zero-resistance non-feedback bridging faults requires two pattern tests.

(2) Demonstrating that detection of some bridging faults requires half-speed flush tests described in Chapter III.

(3) Demonstrating that earlier proposed methods such as IDDQ testing and low power supply voltage testing to increase coverage of resistive bridging faults may not be applicable for designs using 90 nanometer and smaller feature devices.

We also discuss the possibility of achieving complete fault coverage of all realistic bridging faults by appropriate placement and routing of signal lines in the scan cell studied in this work.

The remainder of the chapter is organized as follows. In Section 4.2 we review bridging fault model and test generation for bridging faults. The faults and tests we consider in this analysis report are discussed. In sections 4.3 and 4.4 we give examples of faults that are not detected by existing scan tests. In Section 4.5 we give experimental results and an analysis of the results. Section 4.6 concludes the chapter.

4.2 Preliminaries

In this section we briefly review the bridging fault model and test generation methods for both non-resistance and resistive bridges. The bridging faults internal to a standard scan flip-flop used in an industrial design are described. The tests used for fault detection analysis are also discussed.

4.2.1 Bridging fault model

As the integrated circuit technology improves rapidly, transistor sizes decreased to 90nm and below and the density of the ICs becomes high. New materials and manufacturing processes are being applied. These advances have resulted in shorts and opens to occur most frequently [4.34-4.35]. **Bridging fault model** describes the defects that provide an undesired conducting path between two electrical nodes. They are usually caused by regions with extra conducting material and missing insulating material during manufacturing process. Bridging faults cause functional failures for negligible bridge resistances and timing faults for non-negligible resistances [4.32].

For bridging faults causing hard failures which are sometimes referred to as DC failures or static failures, wired-AND, wired-OR [4.36] and 4-WAY [4.37] bridging fault models are commonly used. Assume A and B are the two faulty nodes involved in the defect. **Wired-AND** bridge model shown in Figure 4-1(a) assumes logic value 0 is presented at both A and B whenever the two lines are driven to the opposite values. Thus there are two faults in such a model: A stuck-at 0 when B is 0 and B stuck-at 0 when A is 0. **Wired-OR** bridging fault model shown in Figure 4-1(b) assumes both A and B have the logic value 1 whenever the two lines are driven to the opposite values. Therefore, the two faults included in this model are: A stuck-at 1 when B is 1 and B stuck-at 1 when A is 1. **4-WAY** bridging fault model assumes that one node dominates the other node by forcing its logic value on the other line. This model includes the faults in both wired-AND and wired-OR models. The detection of a non-feedback negligible resistance

bridging fault needs a single pattern test just like the test for stuck-at fault detection. These bridging fault models can be considered as constrained stuck-at fault model. For example, the faults in a 4-WAY bridge model can be modeled by A stuck-at 0 with the constraining condition B = 0; A stuck-at 1 with the constraint B = 1; B stuck-at 0 with the condition A = 0 and B stuck-at 1 with the constraining condition A = 1.

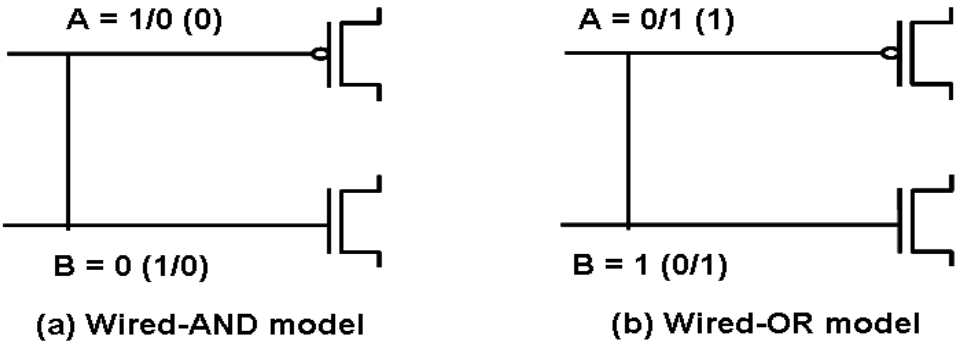


Figure 4-1: Negligible resistance bridging fault models

If there is (at least) one path between A and B through the circuit logic gates, then a bridging fault creates one or more feedback loops. Such a fault is referred to as a **feedback bridging fault** [4.33]. Feedback bridging fault transforms a combinational circuit into a sequential circuit. Therefore, the detection of such bridging faults may require two or more test patterns. The feedback bridging fault is a bridging fault such that both involved leads lie on the same path in the circuit [4.38]. The sensitized loops with an odd number of inversions have the oscillation effects which take place at a frequency much higher than the IC's clock frequency. The oscillation may be propagated to the observable outputs. However, whether the test equipment will detect the fault or not is random since it depends on the exact strobe time of the tester.

It has been found that most of the short defects have significant resistance between the two defective nodes [4.18]. **Resistive bridging fault model** inserts a resistance between the faulty nodes models the short defects more realistically. However, unlike the zero-resistance or negligible resistance bridges, the fault behavior depends on the value of the bridge resistance. As the resistance increases, the fault behavior is weaker and weaker. Intermediate voltages are generated at both faulty lines as shown in Figure 4-2. V1 and V0 will have the same value if the extreme case, zero-resistance bridges, presents. When the bridge resistance increases to infinity, no faulty value is generated. The logic values on the bridged lines depend on the successor gates interpretation and driving gates strengths. Thus, the tests generated using traditional bridging fault models (Wired-AND, Wired-OR and 4-way) may not guarantee the detection of the resistive bridging faults. Many strategies have been developed for resistive bridging fault detection [4.19] [4.24-4.25] [4.28] [4.39]. IDDQ testing we discussed earlier is one option to detect resistive bridging fault. In the presence of short defects, IDDQ caused by fault varies with bridge resistance and depends on the number of transistors included in the Vdd to Vss path. If the current limit used to distinguish between a faulty IDDQ and a fault-free IDDQ is set too high, some faults may not be detected. Conversely, if the current limit is low, a fault-free circuit will be incorrectly indentified to be faulty. Therefore, precise current limit setting is crucial to the IDDQ testing performance. [4.29] investigated IDDQ testability for bridging faults in a variety of flip-flops. It used a static current limit which is derived from bridge resistance values, gain factors for MOSFETs, power supply voltage, threshold voltages and gate to source voltage. It is clear that current limit depends on the resistance values of the bridges. However, the bridge resistance is an unknown factor which varies with technology, material and severity of the defects. Therefore, the current limit is a dynamic parameter. Experimental analysis may help to define more precise current limit.

The resistive bridging fault may also lead to soft failures such as timing delay failures. [4.31] identifies that a few faults producing small transition delays or possibly giving rise to “race” conditions can not be detected by either logic or IDDQ testings.

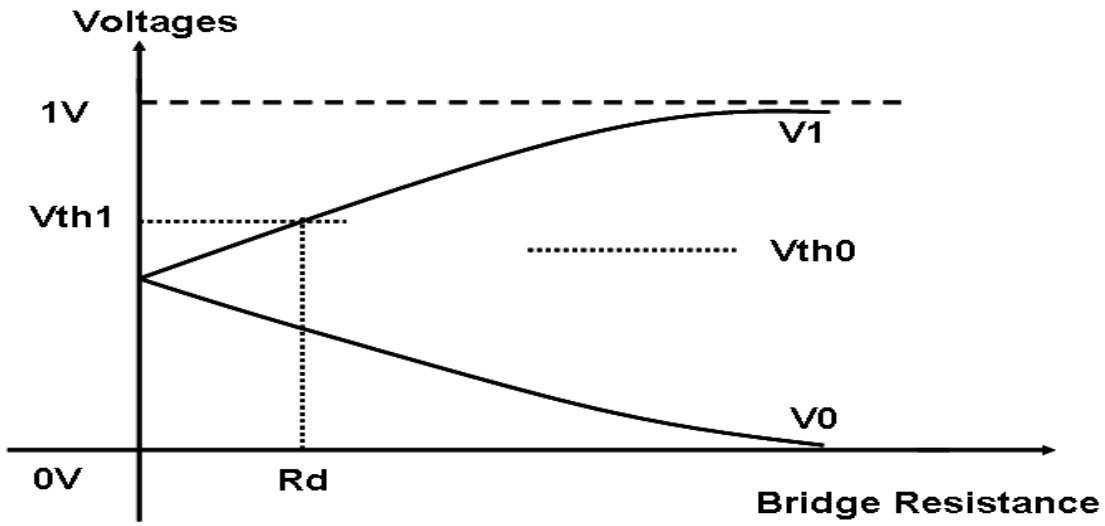


Figure 4-2: Resistive bridging fault behavior

4.2.2 Faults and tests analyzed

The scan cells used in a 90 nanometer industrial design described in Table 1-1 are positive edge triggered MD flip-flops. The number of stuck-at faults in the design is over 60 million and over 27 million faults are in the approximately 614K scan cells in the design. Scan flip-flop presented in Chapter II shows one of the scan cell implementations we studied in this work. However, it should be noted that the observations we derive based on this scan cell also apply to other scan cell implementations.

If bridging faults between every pair of scan cell internal signal nodes are considered, there is a total of 231 faults. We investigated detection of all 231 faults. We

also considered a subset of 29 realistic bridging faults based on the layout of the scan cell. In this chapter, we report experimental results on this set of realistic bridging faults. We investigated the detection of bridging faults with bridge resistances of 10Ω, 100Ω, 500Ω and 1KΩ.

In this work, we considered the existing tests for scan chains which are discussed in Chapter II and flush test 00110011… applied at half-speed. In a half-speed flush test discussed in Chapter III, the flush test is applied at half the frequency at which the scan chain is timing closed.

4.3 Non-feedback zero-resistance bridging faults requiring two pattern tests

Bridging faults cause functional failures for negligible bridge resistances and timing faults for non-negligible resistances [4.32]. Detectable zero-resistance non-feedback bridging faults in combinational logic are known to be detected by single pattern tests [4.33]. However, in scan cells we found that some detectable zero-resistance non-feedback bridging faults require two-pattern tests while others require single pattern tests. Next we give an example of a zero-resistance non-feedback bridging fault whose detection requires a two-pattern test.

Consider the bridging fault D-CPN between nodes D and CPN of the scan cell of Figure 2-1 shown by a line connecting nodes D and CPN in Figure 4-3. Since node CPN does not drive D and vice versa, the fault is a non-feedback bridging fault.

Next we discuss the detection of the D-CPN bridging fault. In order to activate this fault either the condition CPN = 0 and D = 1 or the condition CPN = 1 and D = 0 should be satisfied. From HSPICE simulation, we determined that this bridge behaves as an AND bridge (i.e., if either D or CPN is 0, both nodes behave as logic 0). Consider the first condition. CPN is set to 0 when CP = 1. Both nodes D and CPN behave as 0. However, transistors MP02 and MN02 are turned off when CP = 1. The faulty value D =

0 will not propagate through the faulty circuit. Thus, with the fault activation condition CPN = 0 and D = 1 the fault cannot be detected using a single pattern test. For the fault condition CPN = 1 and D = 0, CPN is set to faulty value 0 due to the bridging fault. The value 0 on CPN is a faulty value only if CP = 0. CP = 0 turns on MP02 and MN02 in the fault-free circuit. Hence, D = 0 will propagate into the master stage if TE = 0 in the fault-free circuit. However, in the faulty circuit, CPN = 0 sets CP1 to 1 and together they turn off MN02 and MP02. Hence, the propagation of D = 0 from the multiplexer to the master stage is blocked. The output of the scan cell will remain at its value set earlier which is not known. Thus, no single pattern test to detect the non-feedback bridging fault D-CPN exists.

Next we show that a two-pattern test can detect the D-CPN bridging fault. In this discussion we refer to the waveforms in Figure 4-4 where solid lines are fault-free waveforms and faulty waveforms are shown in dashed lines. We first initialize node N1 to 1 by applying D = 1 with TE = 0 in clock cycle i. Node N1 gets the logic value 1 at the falling edge in clock cycle i. Next, we set D to 0 in clock cycle i+1. In the fault-free circuit, Din is driven by Vdd through node N19 since D = 0 and TE = 0 turn on transistors MP01B and MP01A, respectively. This will set DP to 0. When CP changes to 0, CP1 and CPN change to 0 and 1, respectively. They turn on MP02 and MN02 and logic value 0 propagates to node N1 at the falling edge of cycle i+1 in the fault-free circuit. This value propagates to output Q when CP changes to 1 in cycle i+2.

However, in the faulty circuit, CPN remains at 0 when CP = 0 in cycle i+1 due to the bridging fault D-CPN. CP1 is then set to 1 since CPN = 0 as shown in Figure 4-4. Hence, transistors MN02 and MP02 are not turned on when CP = 0 in cycle i+1. Therefore, the logic value 0 from DP will not propagate into the master stage (or node N1). N1 will retain the logic value 1 from cycle i in the faulty circuit. The faulty value can be observed at the output Q in cycle i+2. We note that the detection condition of this

bridging fault, D = 10, TI = XX, TE = 00, Q = 10, is a two-pattern test that detects the slow-to-fall transition delay fault at input D.

We also note that the fault discussed above results in functional failure if left undetected. Consider the scenario that a 10 sequence appears at input D in the functional mode of operation where TE = 0. Due to the fault the signal path from the multiplexer to the master stage is blocked when D = 0. The output of the scan cell Q retains the value of 1 since D was at 1 in the previous cycle and this value was propagated to the master stage.

4.4 Detection with half-speed flush test

Next we describe a bridging fault that is detected by the half-speed flush test but not by the same flush test applied at normal-speed. The half-speed flush test [4.10] was introduced in Chapter III. This test ensures that the TI input to a scan cell changes when clock = 1, whereas in normal operation the TI input may change only when clock = 0. As in the case of some stuck-at faults [4.10], some bridging faults not detected by the normal-speed flush tests are detected by the half-speed flush test.

For example, consider the bridging fault DP-N1 indicated by a line connecting nodes DP and N1 shown in Figure 4-5. When CP = 0, transistors MP02 and MN02 are turned on. The logic value on node DP propagates to node N1. It will then propagate to the output when CP = 1 in the fault-free circuit.

If the scan_in (TI) changes when CP = 0 only, in both faulty and fault-free circuit, N1 is getting the value from DP since transistors MN02 and MP02 are turned on. No faulty value will be generated.

However, if TI changes when CP = 1, the output of the multiplexer DP changes within the CP = 1 period. This change will not be propagated to the output in the fault-free circuit since MP02 and MN02 are off when CP = 1. However, in the faulty circuit the change on DP is propagated to N1 due to the DP-N1 bridging fault. The faulty value

on N1 is then propagated to the scan cell output in the faulty circuit. The half-speed flush test ensures that TI changes during the CP = 1 clock phase. Hence, the detection of this fault requires half-speed flush test.

Note that this fault, if left undetected, may lead to an error in the functional mode of operation when the D input of the faulty scan cell changes value during the CP = 1 period.

4.5 Experimental results

In this section we report experimental results on a set of realistic bridging faults extracted from layout. We investigated the detection of bridging faults with bridge resistances of 10Ω, 100Ω, 500Ω and 1KΩ. We used HSPICE for simulations using the tests described in Section 4.2.2. The scan chain was represented by a cascade of three scan cells and the faults were injected one at a time into the second cell.

A bridging fault is modeled by interconnecting two bridged nodes with a resistance between them. Table 4-1 summarizes the simulation results for bridging faults with a negligible bridge resistance of 10Ω. We simulated 29 realistic bridging faults.

The number of faults detected by the normal-speed flush test, with the corresponding percentage is shown in column 2. Column 3 shows the number of additional bridging faults detected by the half-speed flush test. Column 4 shows the number of faults not detected by the flush tests but covered by scan cell boundary SAF/TDF tests. Finally, 3 (10.3%) out of the total 29 bridging faults undetected by Boolean testing are shown in the last column and are discussed further in Section 4.5.1. The detection of 2 (6.9%) faults included in the faults detected by the ATPG generated boundary tests requires two-pattern tests.

In addition, we performed simulations with bridges of different resistance values and the results are discussed in Section 4.5.2.

4.5.1 Undetectable faults analysis

There are 3 bridging faults not detected by Boolean testing. Based on the undetectability reasons, we classify them into two classes.

In the first class, called “same polarity”, the two nodes in the bridging fault are assigned the same values in both clock phases. Figure 4-6 shows the bridging fault N4-Q. When CP = 1 a new value from the output (node MD) of the master stage enters the slave stage and assigns the same value to both N4 and Q through an inverter. When CP changes to 0 both transistors MP07 and MN07 are on. If N4 = 0, MP08 is on and MN12 is on since SD is driven by Vdd. Q is thus driven by Vss. A similar argument applies if N4 = 1. Q and N4 hold the same value in both clock phases. No faulty value can be generated in this case. No functional failure is caused by this class of faults. Thus this fault is redundant.

The faults DP-D and N2-CP are in the other class of undetected faults. This class of faults is Boolean undetected due to the weak strength of the faulty signal. Consider the fault DP-D shown in Figure 4-7, indicated by the line connecting nodes D and DP. First, consider the boundary tests where TE = 0. DP gets the value from input D. In addition, both nodes are located in the multiplexer. Therefore, they have the same value in both the clock phases. The fault is not detected. In the shift mode where TE = 1, both transistors MP01A and MN01B are off. The value on TI propagates to the node DP. In the faulty circuit, the value on D provides the faulty value, which is opposite to the value on TI, to the node DP. In the scan cell we investigated, the driver strength on D is weaker than the one on DP. Therefore, the faulty value cannot be observed.

We note that this fault may be detected with test conditions TI = 0, D = 1, TE = 1 if a strong driver on node D or a weaker driver on DP is used. Similarly, the fault N2-CP can be detected by giving a strong driver for clock signals. However, the fault CP-CP1 will not be detected given strong clock signals. These observations show that we can derive a design rule of applying driver strength, weak or strong, on the boundary nodes of

the scan cell to maximize the coverage of internal bridging faults. Scan cell gets value of TI from the output of the previous cell in the scan chain, the value at D from combinational logic, TE and CP from designed testing signals through different drivers. The strength of drivers may also vary from one scan cell implementation to another in the same scan chain. For example, we can enhance the driver strength of TI by putting two or more inverters in parallel. The design rule can be derived from the simulations and analysis shown above. For the scan cell studied, it needs a stronger driver on D. Drivers on TI, TE and CP can be designed weak or strong. This combination of drivers improves the internal bridging fault coverage by 1/29 (3.4%).

4.5.2 Resistive bridging faults

In Table 4-2, rows 2, 3 and 4 show the simulation results for bridge resistance values of 100Ω, 500Ω and 1KΩ. The fault coverage drops by 3.5% and 13.8% when the bridge resistance goes up to 500Ω and 1KΩ, respectively. The undetected faults are listed in Table 4-3. In order to overcome this coverage loss, two typical methods for resistive bridging fault detection, IDDQ testing and low power supply testing, were investigated.

By simulating a scan cell using HSPICE we measured IDDQ in both clock phases for all additionally undetected faults due to the increase of bridge resistance. The higher IDDQ determined in the two clock phases is used for this analysis. The IDDQ through the transistor affected by a fault is 0.5μA with no defect present and in the range 82.5μA to 373μA in the presence of the fault. For the 90 nanometer industrial product we studied in this work, the faulty IDDQ is less than 0.04% of the nominal total chip IDDQ. Hence, IDDQ testing may not be feasible to cover the high resistance bridging faults for 90nm or beyond.

However, we also note that in the faulty circuit, the transistors on the Vdd to Vss path sink over 100 times more current than in the fault-free circuit. This current surge could be a major reliability issue for these transistors.

An alternative method for resistive bridging fault detection is to lower the supply voltage of the scan cell. The nominal supply voltage for the design is 1V. We performed simulations by applying supply voltages at 0.9V, 0.7V and 0.5V for bridging faults with 1KΩ resistance. Our simulation results show that the supply voltage has to be aggressively lowered to 0.5V from the normal value of 1.0V in order to detect the faults CP1-CP, CP1-Q, CPN-N4 and CPN-Q introduced by increasing the bridge resistance from 100 Ohms (Ω) to 1 kilo-Ohms (KΩ). However, lowering the supply voltage by 50% may not be practical. Therefore, the low supply voltage method may not be applicable for alleviating the coverage loss due to the bridge resistance increase.

4.5.3 Design for test to address undetectable bridging faults

The results presented above show that several bridges are not detected by Boolean or voltage measurement based tests and that other test methods such as IDDQ and low power supply voltage tests may not be feasible in future technologies. To achieve detection of all realistic bridges, one can consider the following strategy. Among all possible bridges between different pairs of nodes in the scan cell, one can determine all the detectable faults. For example in the scan cell considered in this work there are 22 nodes and hence there are a total of 231 pairs of nodes. Out of 231 possible bridges (of 10Ω resistance) we determined that 206 bridges are detectable using Boolean tests. During the design of the scan cell one can attempt to perform place and route such that the undetectable bridges between node pairs are unlikely to occur.

4.6 Conclusions

In this chapter we investigated the detectability of resistive bridging faults internal to scan chains. A complete analysis of bridging faults applying flush tests, a half-speed flush test and ATPG patterns targeting inputs and outputs of the scan cell was presented. It shows that some bridging fault detection needs single pattern tests while detection of other faults requires two-pattern tests even for zero-resistance bridges. The half-speed

flush test improves the fault coverage by about 10.3%. In addition, we observed that an optimized combination of scan cell input driver strengths for the design may improve the fault coverage by 3.4%. We also showed that internal bridging fault coverage drops when the resistance of bridges increases. IDDQ testing and low power supply voltage methods were investigated in order to cover these coverage gaps. We found that these methods may not be feasible for the detection of scan cell internal bridges in the 90 nanometer or beyond industrial products.

Table 4-1: Simulation results for resistance of 10Ω

Total Number of Faults	Normal-speed Flush Test	Half-speed Flush Test	Boundary Tests	Undetected /IDDQ
29 BFs	19 65.6%	3 10.3%	4 13.8%	3 10.3%

Table 4-2: Simulation results for bridge resistances of 100Ω, 500Ω and 1KΩ

	Normal-Speed Flush Tests	Half-Speed Flush Test	Boundary Tests	Undetected/IDDQ detected Faults
100Ω	19 65.6%	3 10.3%	4 13.8%	3 10.3%
500Ω	18 62.1%	3 10.3%	4 13.8%	4 13.8%
1KΩ	15 51.7%	3 10.3%	4 13.8%	7 24.1%

Table 4-3: Undetected faults for bridge resistances of 100Ω, 500Ω and 1KΩ

100Ω	500Ω	1KΩ
DP-D	DP-D	DP-D
N4-Q	N4-Q	N4-Q
N2-CP	N2-CP	N2-CP
	CP-CP1	CP-CP1
		CP1-Q
		CPN-N4
		CPN-Q

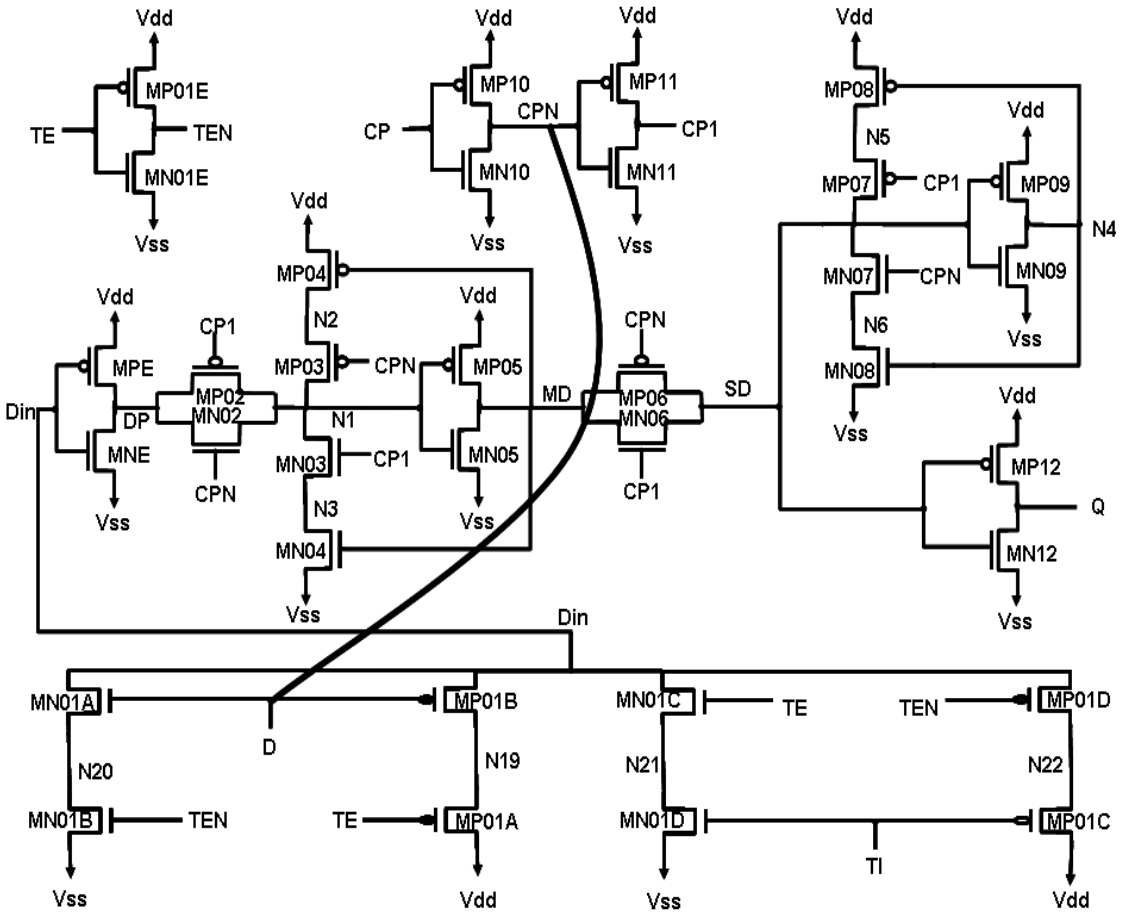


Figure 4-3: Bridging fault D-CPN

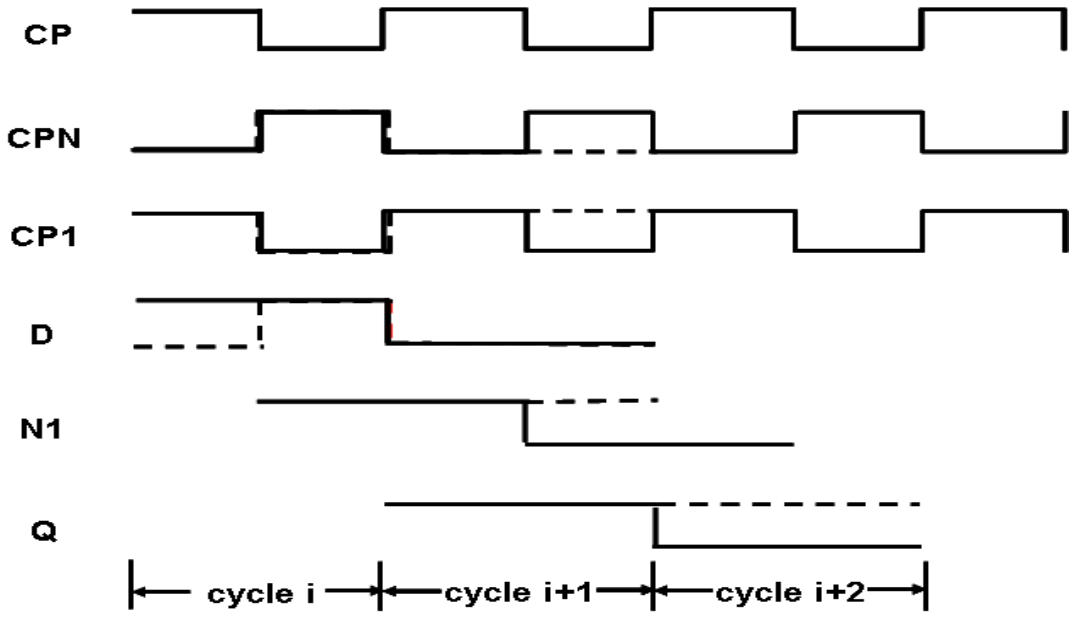


Figure 4-4: Detection of fault D-CPN with two-pattern test

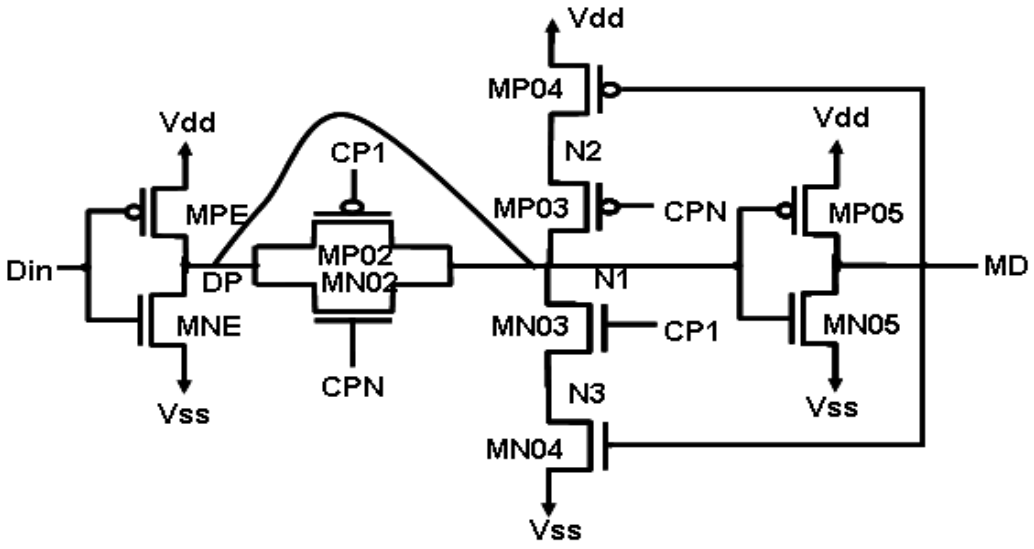


Figure 4-5: Bridging fault DP-N1

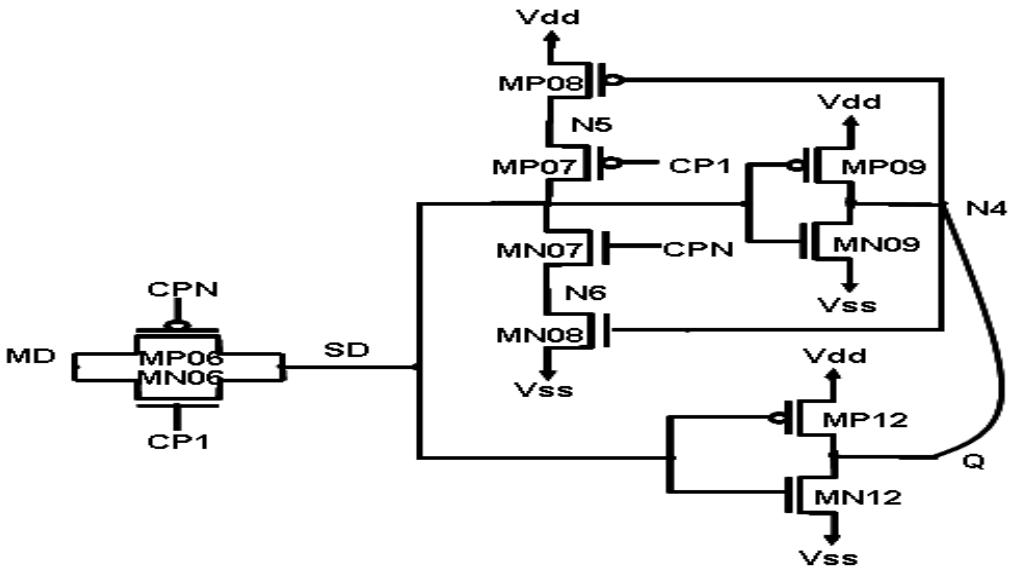


Figure 4-6: Undetected bridging fault N4-Q

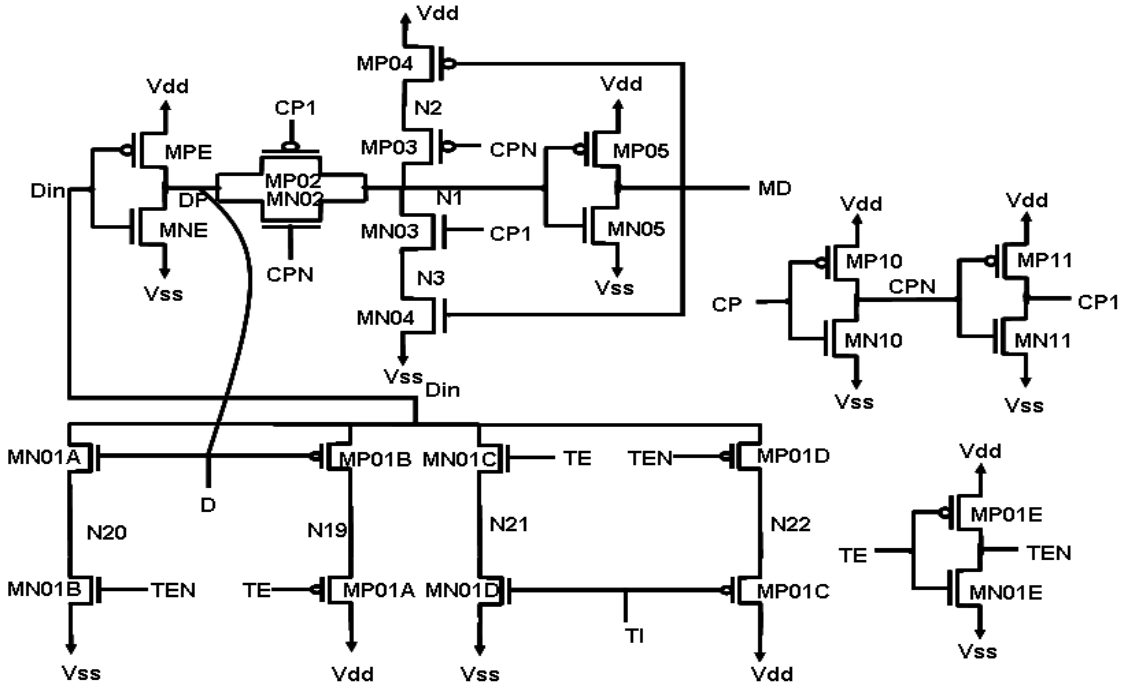


Figure 4-7: Bridging fault DP-D

CHAPTER V NEW TESTS FOR DETECTION OF INTERNAL LARGE RESISTANCE STUCK-OPEN FAULTS IN SCAN CHAIN

In this chapter we investigate the detection of large resistance opens in transistors internal to scan cells. A new flush test and a new method to apply flush tests are proposed to greatly enhance the coverage of opens. In addition, an additional set of ATPG patterns are proposed to detect additional stuck-open faults (SOPs). The proposed tests are shown to achieve the maximum possible coverage of large resistance opens in transistors internal to scan cells. Experimental results on a scan cell used in a 90 nanometer industrial design are included.

5.1 Introduction

In Chapter III and IV we studied the detectability of SAFs, SONs and bridging faults internal to scan cells. In addition to short, break defect is another common defect mechanism in current CMOS ICs. The main reasons of these defects are missing contacts, metal cracks over oxide steps and particles in general. These failure mechanisms will certainly grow with the demand for increasing layout density (smaller contact size etc.). In this chapter, we focus on the detection of high resistance opens in transistors internal to scan cells. A new flush test and a new method to apply flush tests are proposed to greatly enhance the coverage of opens. We also propose new scan based tests to further increase the coverage of opens. The proposed tests are shown to achieve the maximum possible coverage of opens in transistors internal to scan cells. We will quantify them using a 90nm commercial product which consists of approximately 4.3 million cells and 54 million transistors.

The remainder of the chapter is organized as follows. In Section 5.2, stuck-open fault model and test generation for opens are reviewed. In addition, we discuss the open defects we target in our study and review earlier related works. In Section 5.3, we present the proposed set of flush tests and discuss in detail how the proposed tests detect the

targeted opens. In Section 5.4 we propose an additional set of ATPG patterns to detect additional stuck-open faults. In Section 5.5 we give experimental results and an analysis of the results. The undetected opens are discussed. Finally, Section 5.6 concludes the chapter.

5.2 Preliminaries

In this section we review known methods to test for open faults. Since we focus on the large resistance open faults in transistors internal to scan cells in this chapter, the detection of large resistance open faults is also discussed in this section.

5.2.1 Stuck-open fault model

Break defects have been found to be an important contributor to the test escapes [5.1]. **Transistor stuck-open fault (TSOP) model** is common fault model manifesting the physical line breaks happened at the gate, source or drain of the defective transistors. In the stuck-open fault model, a resistance is inserted between the drain, source or gate of the faulty transistor and the node to which it would otherwise be connected in the defect-free circuit as shown in Figure 5-1.

Opens in the terminals of transistors may cause the terminals to float if the open resistance R is an infinite value (in completely open). Detection of open faults in transistors requires two pattern tests [5.13]. The first vector V_1 is applied in order to initialize the circuit to 0 (1). The second test pattern is applied to toggle the state of the circuit from 0 to 1 (1 to 0). In the faulty circuit, the circuit state (observed output) will remain the state from pattern V_1. For example, to detect the gate open of the PMOS in Figure 5-2, the first pattern V1 (a = 1, d = 1) is applied to initialize node F to 0. In the second test pattern V2 (a = 0, d = 0) attempting to set F to 1 activates the open fault. Node F retains the value 0 getting from last test pattern due to the open between nodes a and the gate terminal of the PMOS transistor.

The open faults may be classified by their locations either as a fault at the source/ drain terminal or at the gate terminal of a transistor. If the opens happen at the drain or source of the faulty transistor, the transistor will be permanently turned off. However, the conductivity of the faulty transistor is unpredicted if the open happens at the gate terminal. For example, the gate of a PMOS transistor is open in Figure 5-2. The transistor is turned on if the initial value at gate is 0 and it is off if the initial value is 1. The initial value at gate is not controllable due to the completely open fault. When applying first pattern in Figure 5-2, node F is driven by both Vdd and Vss if the initial value at gate of PMOS is 0. In addition, when applying the second pattern PMOS can be turned on even the open fault presents. Therefore, in order to detect this stuck-open fault, the gate of PMOS is required to be initialized to 1 so that the PMOS remains off when applying the tests. In [5.16], Champac investigated the testability of floating gate defects in sequential circuit. A transistor with a floating gate defect may present some weak conduction for a wide range of realistic situations. In [5.16] the logic and IDDQ testability conditions of floating gate defects in sequential circuit using a realistic defect model is investigated. Large opens are assumed so that any influence of the input signal at the floating gate is considered negligible. Champac also shows that the IDDQ test is applicable for open defects which a low impedance path between the power supply and ground through the defective transistors is created [5.16]. For example, the floating gate fault shown in Figure 5-3 is detected by IDDQ with the detection condition transistor MP03, MP04, MN03 and MN04 on. Note that the assumption for the detection is the gate of MN04 is initialized to 1 and the discharging time is long enough for current detector to make the measurement. Therefore, the IDDQ detectability of floating gate defects depends on technology and topology parameters (e.g. defect parameters, channel width and position of the defective transistor). Hence, the current leakage and the open resistance affect the testability of open faults. To consider open resistance factor in open fault detection, breaks are modeled by resistive stuck-open fault where the open resistance is an unknown

value. In this chapter we focus on large resistance open faults. Detection of variable resistance open faults will be considered in the next chapter.

5.2.2 Open faults studied

In this work, we consider the drain, source and gate open faults of each transistor inside a scan cell. In the scan cell we studied in Figure 2-1, there are a total of 34 transistors and hence we consider 102 stuck-open faults.

The large resistance stuck-open fault model shown in Figure 5-4 is used in this work. Considering the open shown in Figure 5-4(a), the faulty node F can be set to 1 (0) if we keep node c at 1(0) for long enough time. The length of time required varies for different transistors and also depends on the resistance inserted. We derived these values from simulation.

Detection of opens in transistors requires two pattern tests [5.13]. Opens in the gate terminals of transistors may cause the gate terminal to float if the open is an infinite resistance open. A floating gate may have an intermediate voltage making the affected transistor to conduct weakly [5.14-5.16]. Detecting such opens may require I_{DDQ} based tests [5.14-5.16], or they can be detected using tests for transistor stuck-on faults. In this work, we consider only finite resistance opens and detection by logic or voltage measurement based tests. If the resistance of the open is not large, then the effect of the open will be to increase the delay of the affected scan cell. Such opens may require delay tests targeting small delay defects [5.17]. In this chapter, we consider only large resistance opens that cause gross delay defects. Such opens were considered in [5.3] and [5.18]. In [5.3], methods to add transistors such that all the opens in the scan cell are detected by appropriate two pattern tests were described. However, these methods increase the size of the scan cells and hence may not be practical. In [5.18], methods to design scan cells were proposed such that the probability of occurrence of undetectable opens is minimized. These methods do not increase the size of the scan cell and also do

not affect the performance. However, the methods leave some opens undetected by the standard flush tests and scan cell boundary tests for SAFs and TDFs. In this chapter, we consider enhancing flush tests and ATPG generated tests such that all the detectable high resistance opens are detected. The opens that are not detected are one of the two parallel transistors open in a CMOS transmission gate. Such faults can only be detected, if at all, by tests that can detect small delay faults [5.3].

5.3 Scan stuck-open flush tests

In this section, we define a new combination of flush tests called *scan stuck-open flush tests* along with a new stuck-open ATPG test set to improve the coverage of large resistance SOPs. We found that the proposed tests guarantee the detection of all such opens other than those in the transmission gates that control the data propagation from the multiplexer to the master latch or from the master latch to the slave latch. Analysis of the proposed tests is given next together with a discussion of the faults additionally detected. Next we describe the tests.

As noted earlier, traditionally the three flush tests 00…0, 11…1 and 11001100… described earlier are applied in arbitrary order. We propose to apply six flush tests shown in Table 5-1. The first three tests are the same as the traditional tests with the following restrictions. The three flush tests are applied in the order given in Table 5-1. Additionally, after scanning in the third flush test 00110011… the scan clock is changed to 1 and held in that state for M clock cycles. This is followed by scanning in the fourth test 00110011…. After the fourth test is scanned in, the scan clock is changed to zero and held in this state for N cycles followed by scanning in a new flush test 0101… at half speed. Finally, we scan in two additional bits 01 for even number of scan cells or 10 for odd number of scan cells in the scan chain at very low frequency. Assume that the scan chains are closed at 10 nanoseconds. Half-speed flush test is thus applied with clock period of 20 nanoseconds. Normal speed flush tests are applied at 100 mega Hertz. The

value of the time to hold the clock lines at 1 and 0 is experimentally determined, and a duration of 15 cycles is found to be adequate for the scan cells (c.f. Figure 2-1) described in Chapter II. An adequate clock period for the last two bits shifted is determined to be 1 microsecond for the scan cells under consideration.

In the following subsections we will discuss in detail each step of the proposed scan stuck-open flush tests. An important issue we discuss is the usefulness of detecting the additional faults that are not detected by the traditional tests. A fault is meaningful if left undetected it can either affect the functionality in the native mode of operation or pose a reliability risk.

Table 5-1: Scan stuck-open flush tests

Tests	Comments
11…1	Flush tests in this designated order
00…0	
00110011…	
Hold clock signal at 1 for M cycles	Flush test after pre-charging clock lines to 1
00110011…	
Hold clock signal at 0 for N cycles	Half-speed flush test after pre-charging clock lines to 0
Half-speed flush test 0101…	
Applying 01 slow for 2 clock cycles	Slow speed flush test

5.3.1 Flush tests in the designated order

Before we load the flush tests into the scan chain, the initial values stored in the scan cells are unknown. Therefore, the initial value on a faulty node is undetermined (when the first test is applied) if the flush tests 00…0, 11…1 and 00110011… are applied in a random order. We observe that some additional large resistance SOPs are detected if we run the sequence of these tests with appropriate initial conditions applied to the faulty nodes. To obtain such detections, we order the tests to initialize the faulty nodes. Specifically applying TI = 1 or 0 for multiple clock cycles using the flush tests 11…1 and

00…0 was found to result in detection of additional SOPs. An example of one such fault is given next.

Consider the gate of MP05 (node N1) stuck-open highlighted by an arrow in Figure 5-5. The faulty node is denoted by F. In order to detect this fault, we want to pre-charge node F to 1 by applying a 1 to node N1 over many cycles. Applying TI = 0, N1 is set to 0 when CP = 0. It will turn MP05 on in the fault-free circuit. Node MD is then driven by Vdd. However, in the faulty circuit, F is driven through a large resistance and hence retains its initial value 1. It discharges slowly when N1 is set to 0 by applying TI = 0. The transistor MP05 will remain off and the node MD cannot be driven by Vdd. Thus, the value 1 cannot be stored at MD. This can be accomplished by scanning multiple 1s followed by a 0 through the input pin TI. Applying multiple 1s helps to initialize MD to 0 and charges F to 1 as well. Next, TI = 0 is scanned in. MD retains its value of 0 from the previous cycle instead of 1 in the fault-free circuit. Note that we may observe the fault-free value after applying multiple TI = 0s since they keep N1 at 0 and discharge F to 0 finally. However, if the open resistance is large enough such that the length of time of discharging F to turn on MP05 is longer than half the clock cycle, we can still capture the faulty value after we first apply TI = 0. Waveforms in Figure 5-6(a) show the detection of this fault with initial value on node F = 1. Figure 5-6(b) shows that the fault is not detected with initial value 0 on the faulty node F.

Similarly, the stuck-open fault on SD of MP12 denoted by F1 in Figure 5-5 is detected by scanning multiple 0s followed by TI = 1.

Since scan chain consists of a large number of scan cells it can be safely assumed that applying the flush tests 11…1 and 00…0 will be enough to initialize the faulty nodes. Accordingly, we apply the flush tests in the following order: apply flush tests 11…1 followed by 00…0 and then shift the test 00110011… into the scan chain. Applying 11…1 will initialize the faulty nodes for the fault detection that needs multiple TI = 1s. Next, by applying the 00…0 test, we generate the 1 to 0 transition necessary to

detect the faults while at the same time the internal nodes are initialized for fault detection requiring multiple TI = 0s. Finally, the flush test 00110011… is applied to detect additional faults.

Note that the faults illustrated in Figure 5-5 can affect the functional mode of operation and therefore it is important to detect them. For example, consider the fault where the gate of MP05 is open in the scenario where, during functional mode, a long sequence of 1s appears at the D input. This will charge up the faulty node. When a 0 appears at D in a subsequent clock cycle the output will be faulty.

We also note that traditional flush tests do not guarantee detecting all these faults. For example, the three flush tests running in the order 00110011… and 00…0 followed by 11…1 misses the fault where the gate of MP05 is open.

5.3.2 Flush testing after holding the clock signal at 0 or 1 for a duration of several clock cycles

As discussed above, stuck-open faults located on internal data signal nodes can be detected with proper initial conditions. We also observe that detection of some large resistance SOPs requires specific initial state of clock signal (CP) before applying flush tests.

For example, Figure 5-7 shows the master and slave latches of a MD flip-flop with the gate of MN02 (node CPN) stuck-open. The fault site is highlighted by an arrow and F denotes the faulty node. In the fault-free circuit, node F is connected to CPN. In the faulty circuit if the gate of MN02 (F) has initial value 1, MN02 is on. Applying half-speed flush test, TI changing when CP = 1 will not propagate to the output Q in the fault-free circuit, since MN02 and MP02 are off (as discussed earlier half-speed flush test insures that TI changes when CP = 1 for all scan cells). However, in the faulty circuit, MN02 remains on since F is being driven through a large resistance (due to the fault) and the value 1 on node F discharges slowly. Note that the open resistance is assumed large

enough such that the first change in TI is propagated into the master stage before F is discharged to turn off MN02. Therefore, changes in TI when CP = 1 will propagate to the output Q. This is shown in Figure 5-8(a), where solid lines are signals from the fault-free circuit and dashed lines show faulty waveforms.

If node F has an initial value 0 instead, MN02 will behave as stuck-off. Assume MP02 operates normally. The value on node DP can enter node N1 and propagate to the output only when CP = 0. Waveforms in Figure 5-8(b) show that this fault is not detected. Therefore, this fault is detected by the half-speed flush test if the gate of MN02 has been initialized to logic value 1. To enable the detection of this fault, we need to hold the clock signal at 0 for a certain period of time in order to charge the node F to 1 before applying half-speed flush test.

Another example shown in Figure 5-9 is a SOP on the gate of transistor MN06 (denoted as F). The detection of this fault requires holding clock at 1 to charge node F to 1 before applying the normal speed flush test. We refer to Figure 5-9 and Figure 5-10 in the following discussion. When CP = 0, CP1 is 0 and transistor MN06 is turned off in the fault-free circuit. Changes in TI within CP = 0 in clock cycle i will not propagate to the output Q. However, if F is pre-charged to 1 it discharges slowly when CP1 = 0. In the faulty circuit, MN06 is on when CP = 0. In clock cycle i, TI changes from 1 to 0. This change propagates to Q through the transistors MP02, MN02 and MN06. The faulty value 0 is observed at the next rising edge of the clock as shown in Figure 5-10(a). Similarly, this fault is also detected when TI changes while CP = 1 as shown in the clock cycle i+2. Figure 5-10(b) shows that the fault is not detected with F initialized to 0.

When applying the flush tests, clock can start with either 0 or 1 and then change state after half a clock cycle. However, we can pre-charge the clock lines by holding CP at the required initial state for a proper length of time. After that, we can apply the flush test for detection. To detect the gate of MN02 stuck-open fault discussed above, clock is

held at 0 for a certain period of time. It helps to charge the faulty node F to 0. Then the half-speed flush test is applied for detection.

The above examples of fault detection motivated us to add two additional flush tests after applying 11…1, 00…0 and the first 00110011… in designated order. We add a normal flush test 00110011… after holding the clock lines at 1 for M clock cycles. Since no additional fault is detected by half-speed flush test with initial condition clock = 0, we use normal speed flush test in order to avoid increasing test application time. It is important to note that this test can not be merged into the last normal speed flush test 00110011…. The first 00110011… sequence is applied for detection of faults that are initialized by the flush test 00…0. If we held the clock signal at 1 for M cycles before we apply this test, those initialized signals would lose their values and some faults will be missed thereafter. For example, SOP on source or drain of MP12 shown in Figure 5-5 is detected by applying 00…0 followed by flush test 00110011…. Flush test 00…0 helps to charge F1 to 1. When TI = 1 sets SD to 0, F1 discharges slowly. Thus Q can not be driven by Vdd. If clock signal was held for M cycles, F1 would discharge to 0 and the fault cannot be detected.

After the second application of the test 00110011…, the clock signal is held at 0 for another N clock cycles followed by the half-speed flush test 0101…. Other half-speed flush tests like 00110011… also detect these faults. However, we use the test 0101… here to reduce the time required to apply the last flush test pattern. As given in Table 5-1, this test consists of shifting in the bits 01 at very slow speed. The details of this slow test are discussed in Section 5.3.3. We note that high switching activity in scan chains could be caused by using the flush test 0101… compared to that caused by the flush test 00110011…. In case the higher switching activity is unacceptable one can replace the flush test 0101…with the flush test 00110011…. In the latter case the last flush test in Table 5-1 should be changed to a five bit sequence 00110. This issue is discussed in the next section.

It is important to note that some of the faults discussed above affect the functional mode behavior and therefore it is important to detect them. In the functional mode, clock may be shut down to save active power. Consider the scenario that the clock is turned off when clock = 0, it charges CPN to 1. When clock is powered on again and D changes its value when clock = 1, the output will be faulty due to the SOP on gate of MN02.

5.3.3 Flush test with very slow clocks

Many SOPs located in the slave and master stages are not detected by normal flush tests since the output of the slave or the master stage retains its value from the previous half clock cycle. By giving enough time, the nodes will discharge and the faulty value will be generated thereafter. To take advantage of this we will run a test at very low frequency but only for a few clock cycles. This test is equivalent to data retention tests [5.18].

Consider the SOP located on the drain/source of transistor MP08 (node N5) shown in Figure 5-11. When CP = 1, logic value 1 enters the slave stage at node SD, N4 = 0 and output Q = 0 since transistors MP06 and MN06 are on. When CP switches to low, N5 is driven by Vdd since MP08 is on in the fault-free circuit. Hence N5 and Q hold logic value 1 and 0. In the faulty circuit, SD is floating when CP = 0 but still retains a value 1 from the last half cycle (when CP = 1) since SD discharge slowly (assume the open resistance between N5 and F is large enough such that the rate of charging SD is lower than the discharging rate). Thus, Q will remain at 0. No faulty value is generated. However, if we run the tests slow enough to let the value on node SD discharge to 0, N4 and Q will change to faulty value 1. MP08 is then turned off while MN08 is on. This fault is detected. Thus, to detect this fault we set Din to 1 and apply one slow clock cycle.

Similarly, to detect N2 of transistor MP04 stuck-open we need to set Din to 0 and apply one slow clock cycle. Thus, to detect all such faults we have to set Din to 0, 1 and apply one slow clock cycle each time.

Makar and McCluskey in [5.8] proposed that running tests at clock period of 10 microseconds will detect these SOPs. For our scan cell implementation, test running at clock period of 1 millisecond is slow enough to detect these faults. However, this poses test cost problems. Running flush tests for a scan chain containing thousands or more scan cells at 1 mega Hertz or a clock period of 1 microsecond takes over 1 millisecond which is not cost effective.

Instead, we propose a new test to detect these faults. We first load the scan chain with the flush test 0101…. Consider two scan flip-flops X, Y such that Din of X (Y) is set to 1 (0). We apply a slow clock with scan_in = 0. This detects faults N5 of MP08 stuck-open in X and fault N2 of MP04 stuck-open in Y. The slow clock sets Din of X (Y) to 0 (1). If we next apply one more slow clock with scan_in = 1 then N2 of MP04 SOP in X and SOP on N5 of MP08 in Y are detected. Thus, this test will detect all such detectable faults. To optimize test application time, we merge this test with the last half-speed flush test as discussed earlier.

Note that if the last half-speed flush test used is 00110011… instead of 0101…, in order to set Din in each scan cell of scan chain to both 0 and 1 we need to apply the low frequency test using 5-bits 00110.

Note that the faults discussed above can also affect the functional mode of operation. Consider the fault N5 of MP08 stuck-open. When clock is shut-off during clock gating, SD is floating. If SD was set to 1 prior to this then the fault will appear when we get out from the clock gating phase. This is a problem if state retention is required. Frequency scaling is another scenario when such faults could manifest themselves.

5.4 ATPG generated stuck-open tests

In addition to the standard scan cell boundary tests for SAFs and TDFs, we propose an additional set of ATPG patterns shown in Table 5-2 to detect additional SOPs.

In Table 5-2, we show the states of the scan cell inputs D, TI, TE as well as the fault-free scan cell outputs for the two pattern tests used to detect additional large resistance SOPs. It should be noted that these patterns require either 0 to 1 or 1 to 0 transitions on the test enable signal TE.

Flush tests are applied with test enable signal TE steady at 1. Two pattern tests to detect TDFs are applied with TE = 0 if broadside tests are used and TE changing from 1 to 0 if skewed load tests are used. There is no two pattern tests are applied with TE changing from 0 to 1. However, we found that the detection of some SOPs requires transition of TE from 0 to 1. We propose a new set of ATPG patterns including 0 to 1 transition of TE to detect these SOPs. For the sake of completeness, in this set we also include the tests that use 1 to 0 transitions on TE. There are two groups of faults. Both these groups of SOPs require a two pattern ATPG generated test. However, in one case the initialization happens in the last shift clock when TE = 1. The second pattern requires TE = 0. This requires a transition on TE from 1 to 0. For the second group the initialization occurs when TE = 0 and the second vector of the two pattern test requires TE = 1. Thus it requires a transition of TE from 0 to 1.

Table 5-2: Additional stuck-open ATPG tests

D = X1, TI = 0X, TE = 10, Q = 01
D = X0, TI = 1X, TE = 10, Q = 10
D = 1X, TI = X0, TE = 01, Q = 10
D = 0X, TI = X1, TE = 01, Q = 01

5.4.1 Stuck-open faults detection requiring TE = 10

In order to detect SOP on the drain/source of MP01E shown in Figure 5-12 the test must satisfy D = X1, TI = 0X, TE = 10, Q = 01, where X is a “do not care”. The

faulty node is denoted by F in Figure 5-12. We will refer to Figure 5-12 and waveforms in Figure 5-13 in the following discussion. In the clock cycle i, TE is set to 1 initializing TEN = 0. Transistors MN01C and MP01D are on. TI = 0 turns MP01C on and initializes Din to 1 in clock cycle i and propagates to Q at the next clock signal rising edge. No faulty value at Q is observed in the clock cycle i+1. When TE switches to 0 in the clock cycle i+1 TEN is set to 1 in the fault-free circuit. Hence transistor MN01B is turned on. D = 1 in cycle i+1 turns MN01A on and sets Din = 0 in the fault-free circuit. However, in the faulty circuit, if open resistance is large enough, TEN will remain at 0 from last clock cycle since source/drain F of MP01E is open. It turns MN01B off and MP01D on. If TI = 1, MN01D is turned on and MN01C is off since TE = 1. In addition, D = 1 turns MN01A on but MN01B is off due to the fault. Din is floating but retains 0 from clock cycle i. If TI = 0, it turns MP01C on and MP01D is on due to the fault. Din is thus driven by Vdd through node N22. Din will hold value 1 as well as the case of TI = 1. Therefore, no matter TI is 0 or 1 faulty value 1 is generated at Din. It will be propagated to the master stage when CP = 0 in the clock cycle i+1. The faulty output 0 can be observed in the next clock cycle at Q.

Consider a segment of scan chain with three scan cells cascaded shown in Figure 5-14. Assume that the fault shown above is present in the second scan cell. The test condition for the fault discussed above is D1 = X1, TI1 = 0X, TE = 10, Q1 = 01. This can be accomplished by ATPG targeting bridging fault D1-Q1. One of the two tests for this bridging fault is setting logic values 0 and 1 to output pin of the faulty scan cell Q1 and input pin D1 when TE = 0. In order to set Q1 = 0, ATPG applies TI1 = 0 in the previous clock cycle where TE = 1. It initializes the node Din to 1. When TE switches to 0, D1 is set to 1. In the fault-free circuit, Din = 0 when CP = 0 and Q1 is set to 1 one clock cycle after. However, in the faulty circuit, Din retains value 1 from previous cycle. We will observe the faulty value 0 at Q1 as discussed previously. Note that these SOPs may be potentially detected by other ATPG tests.

Note that detection of this fault is important since it may result in functional failure. Consider the scenario that logic value 1 appears at D1 in functional mode operation where TE = 0. TEN is floating due to the fault. It could be set to either 1 or 0 based on the switching activity in its neighborhood. If TEN gets set to 0, we can not set Din to 0 since MN01B is off. The output of this scan cell therefore can not be set to 1 and will cause intermittent failure during functional mode operation.

5.4.2 Stuck-open faults detection requiring TE = 01

There is another group of SOPs that requires TE = 01 transition for detection. These are highlighted by arrows in Figure 5-15. For example, the stuck-open on the drain of MN01E is denoted by F1. The test condition is D = 1X, TI = X0, TE = 01, Q = 10. Transferring to the second cell in Figure 5-14, it is D1 = 1X, TI1 = X0, TE = 01, Q1 = 10. A test targeting bridging fault D0-D1 satisfies this condition. If the test D0 = 0, D1 = 1 is applied in the capture cycle TE = 0, Q0 and Q1 are set to 0 and 1 when TE switches to 1 (shifting out mode). This satisfied the first pattern in the test D1 = 1, TI1 = X, TE = 0. TI1 gets value 0 from Q0 when TE = 1. The second pattern D1 = X, TI1 = 0, TE = 1 is satisfied. Therefore, this test detects the SOP deterministically.

5.5 Experimental results

To determine the large resistance SOP coverage by the tests proposed, we simulated a scan chain using HSPICE. We used a segment of a scan chain with three scan cells shown in Figure 5-14. A large resistance SOP was modeled by inserting a 100 mega-ohm resistor in the fault site. A target fault is injected into the second scan flip-flop by modifying its circuit description. For the 90 nanometer design discussed in Chapter I, the scan chain timing closure was at scan shift cycle of 10 nanoseconds. Thus, for half-speed flush tests, the shift cycle time of 20 nanoseconds was used. We also determined that holding the clock at 1 or 0 to pre-charge clock lines was achieved by holding the

clock for 150 nanoseconds. The slow speed two bits flush test was applied at a shift cycle time of 1 microsecond.

Table 5-3 summarizes the simulation results. As discussed earlier, a total of 102 SOPs reside in a single scan cell shown in Figure 2-1. The number of faults detected by the new scan stuck-open flush test, with the corresponding percentage, is shown in column 2 of Table 5-3. Note that the traditional flush tests, 00…0, 11…1 and 00110011…, applied in arbitrary order only ensure that 37 (36.3%) SOPs are detected. They are included in the 74 SOPs detected by scan stuck-open flush tests. Column 3 shows the number of SOPs not detected by the flush test but detected by scan cell boundary TDF tests. Column 4 shows the number of faults detected by the stuck-open ATPG tests shown in Table 5-2. These faults are highlighted by arrows in Figure 5-12 and Figure 5-15. The remaining 8 faults are not detected by Boolean testing. Next, we discuss the undetected faults.

The last column of Table 5-3 shows that 8 (7.9%) SOPs remain undetected. They are drain and source stuck-open faults located on transistors MN02, MP02, MN06 and MP06 highlighted by arrows in Figure 5-16. These SOPs are undetected since they are in one of the two transistors in the transmission gates that control the propagation of signals from the multiplexer to the master stage or from the master stage to the slave stage. Open transistor faults in CMOS transmission gates can only be detected, if at all, by delay fault tests [5.3]. One way to handle these faults is to use a single double sized NFET in a transmission gate as suggested in [5.18]. If this is done, then all stuck-open faults in the scan cell will be detected by the tests proposed in this work.

5.6 Conclusions

In this chapter, we investigated the detectability of scan cell internal large resistance stuck-open faults. An analysis of large resistance SOPs in a scan cell under flush tests and boundary SAF/TDF tests was presented. A new scan stuck-open flush test

was defined based on the flush tests typically used. In addition, a new set of ATPG generated tests was also presented. Together, these tests detect all detectable large resistance stuck-open faults.

Table 5-3: Experiment summary of stuck-open faults detected

Test	Scan Stuck-open Flush Tests	Boundary SAF/TDF Tests	Stuck-open ATPG Tests	Undetected Faults
# of Faults	74 (72.5%)	10 (9.8%)	10 (9.8%)	8 (7.9%)

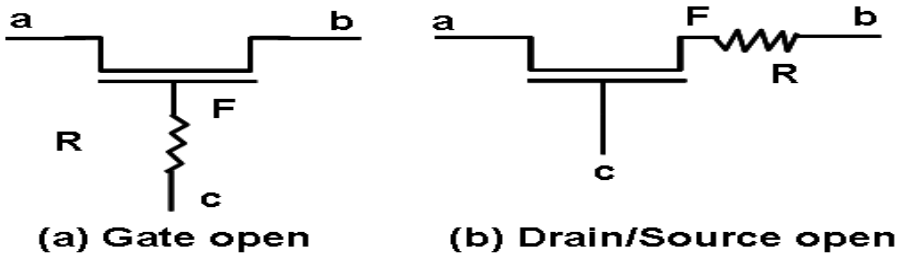


Figure 5-1: Transistor stuck-open fault model

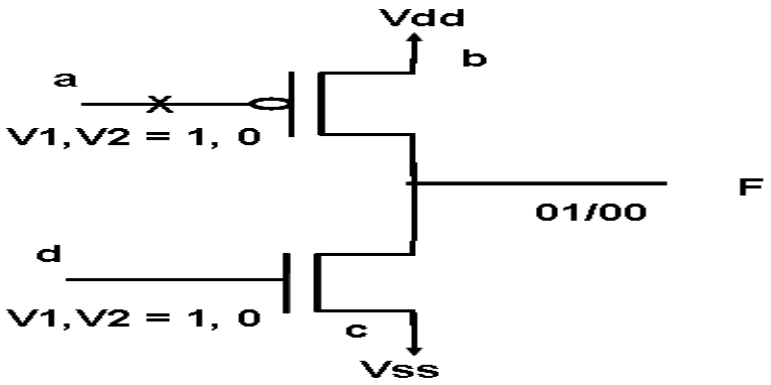


Figure 5-2: Stuck-open at gate of transistor

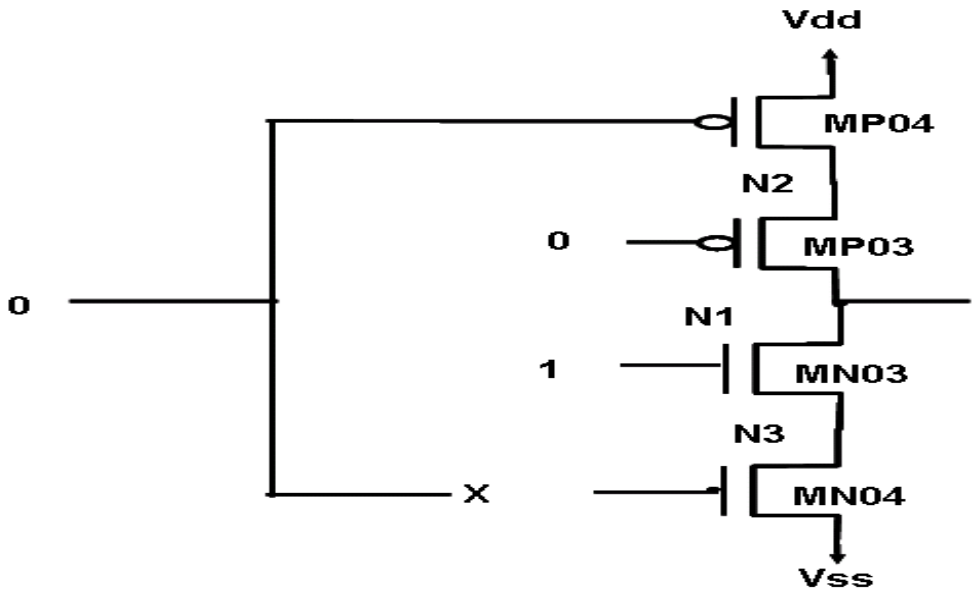


Figure 5-3: IDDQ detectable floating gate defects

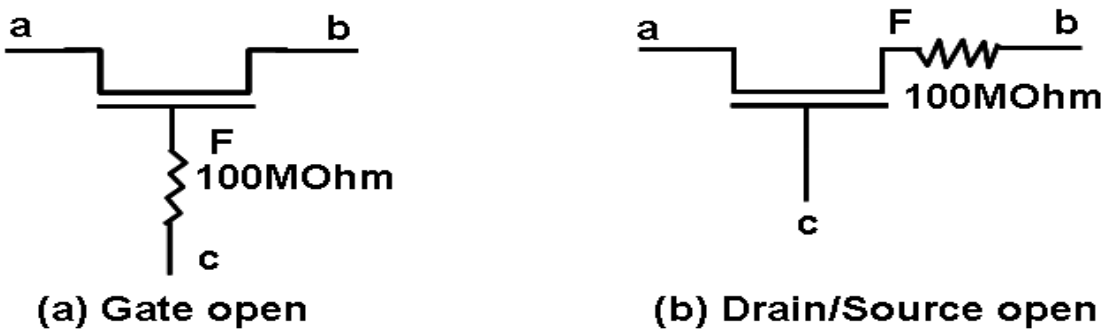


Figure 5-4: Large resistance stuck-open fault model considered in Chapter V

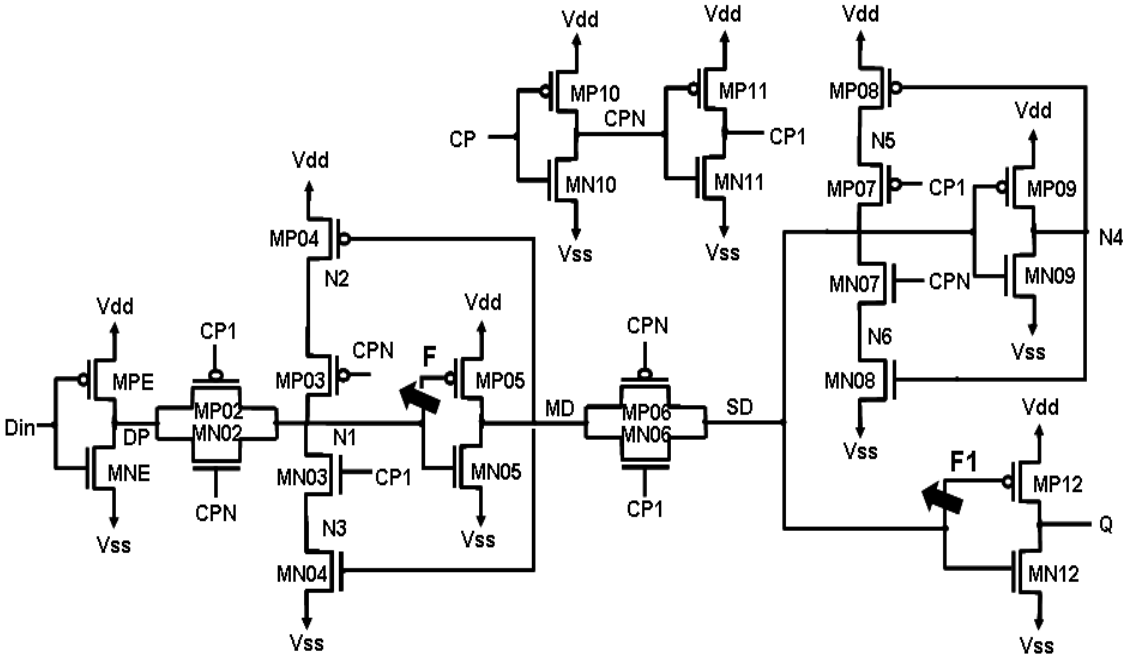
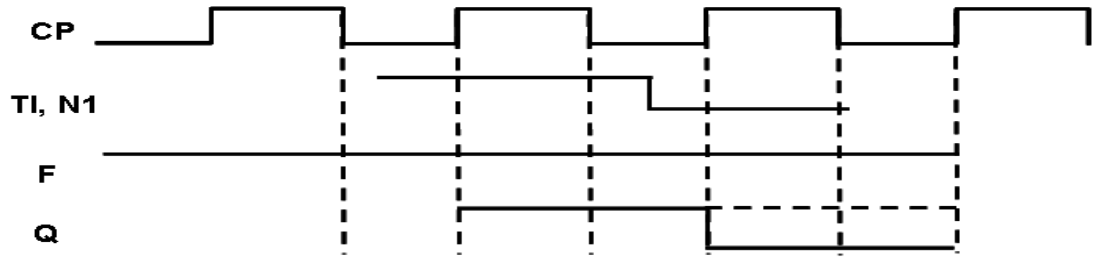
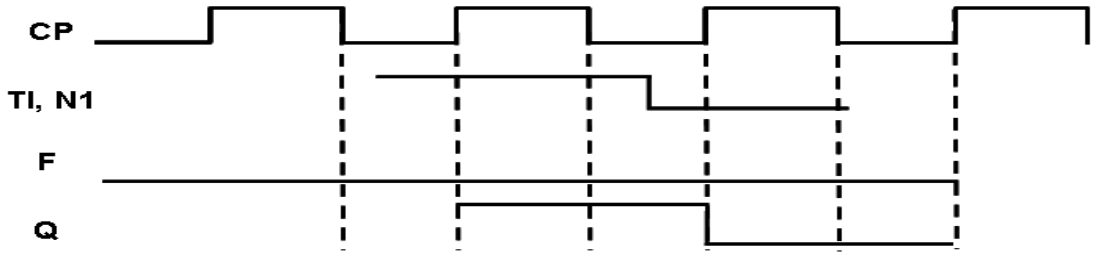


Figure 5-5: Gate of transistor MP05 and MP12 stuck-open



(a) Fault detected with initial value of F = 1



(b) Fault undetected with initial value of F = 0

Figure 5-6: Detection of transistor MP05 gate stuck-open

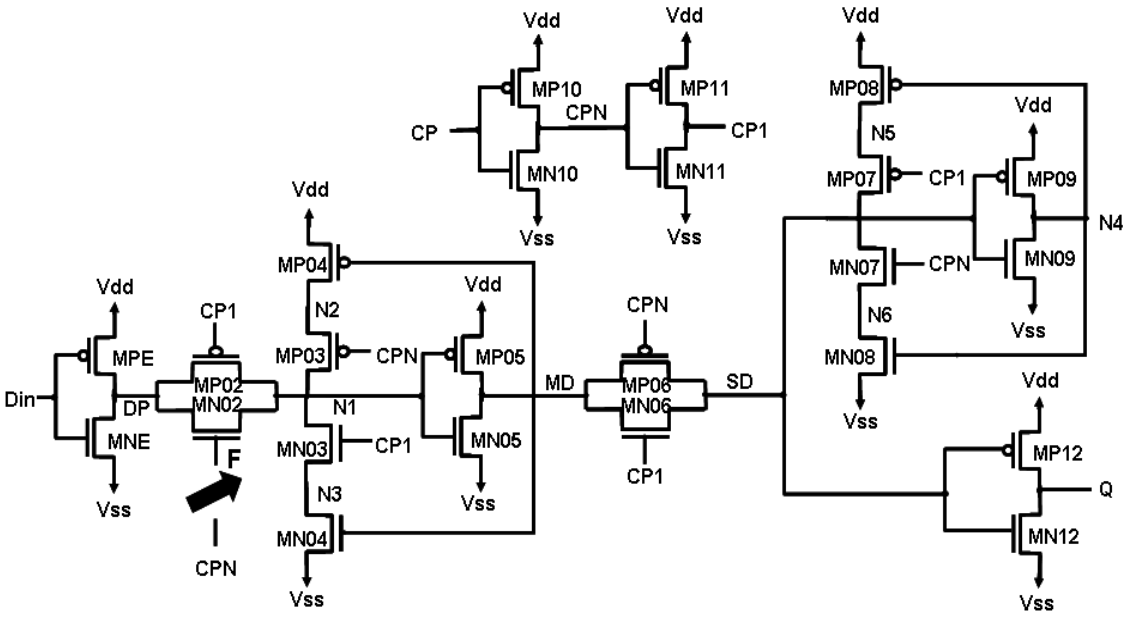


Figure 5-7: Gate of transistor MN02 stuck-open

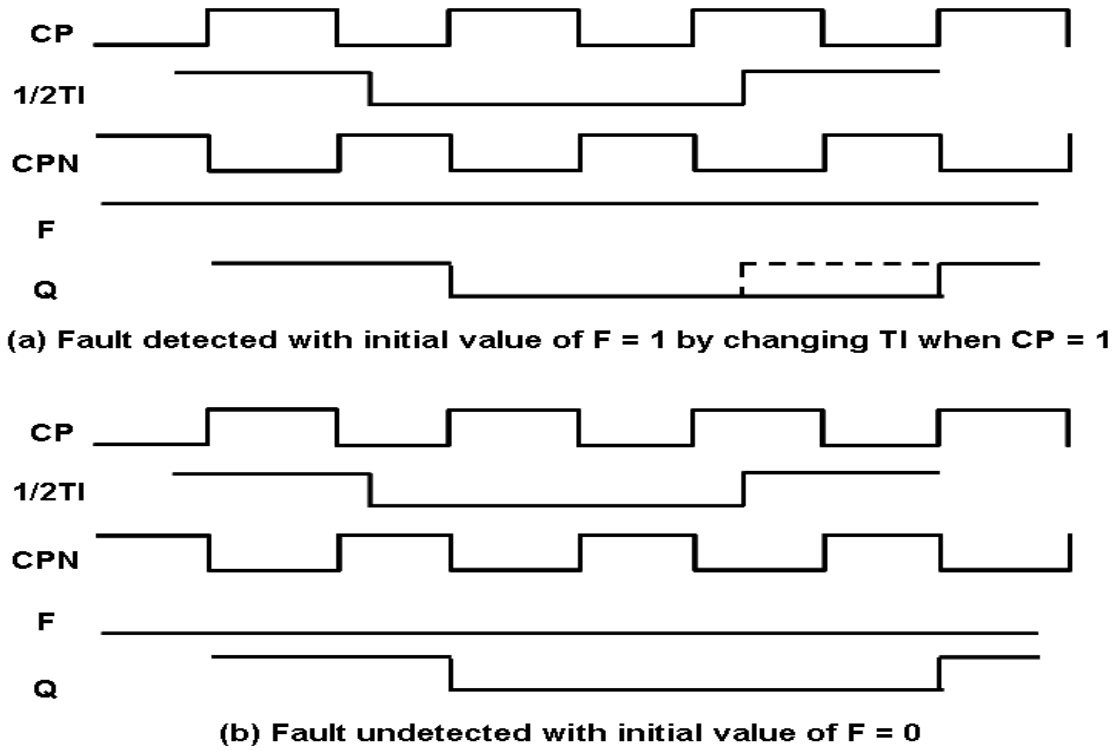


Figure 5-8: Detection of transistor MN02 gate stuck-open

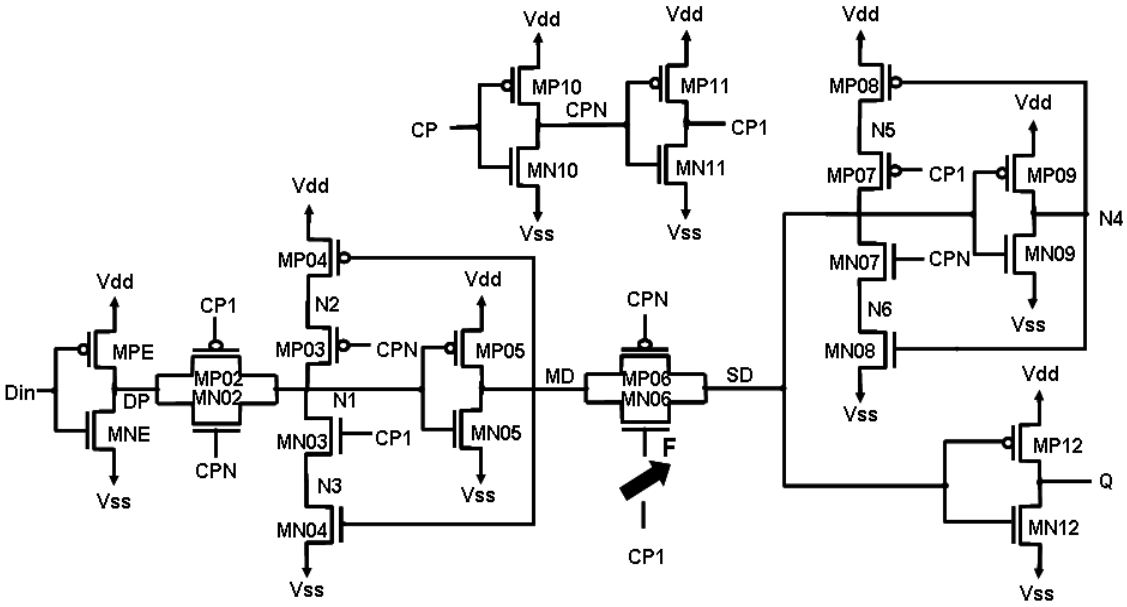


Figure 5-9: Gate of transistor MN06 stuck-open

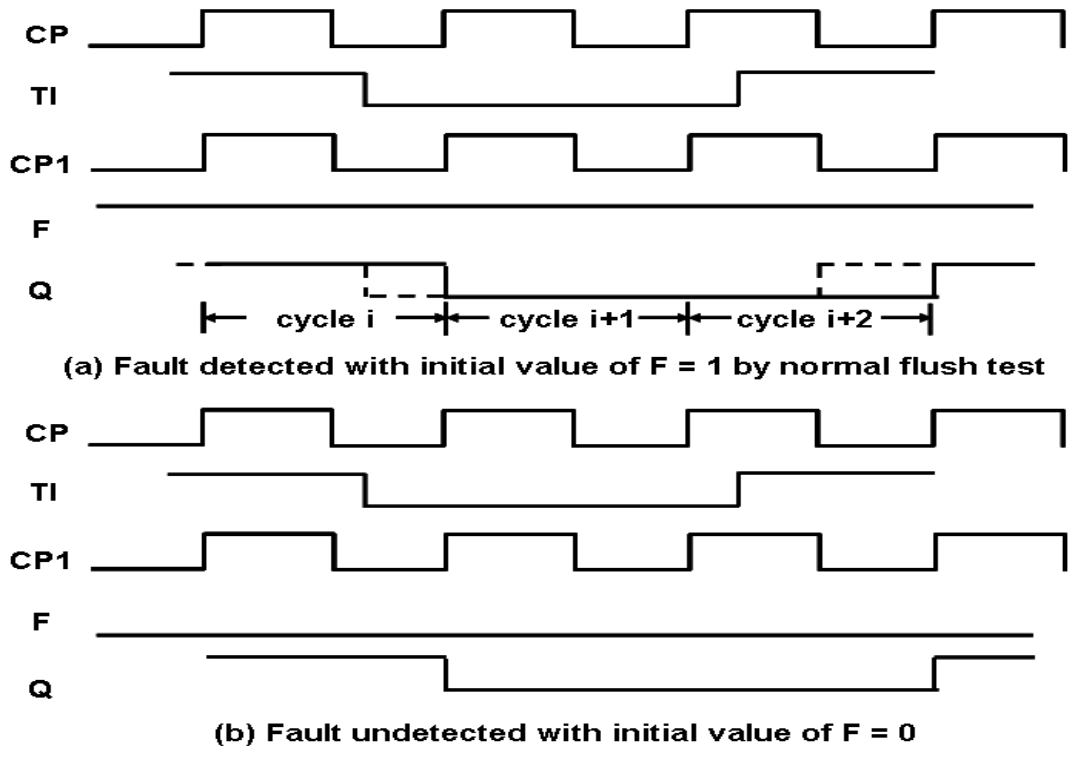


Figure 5-10: Detection of transistor MN06 gate stuck-open

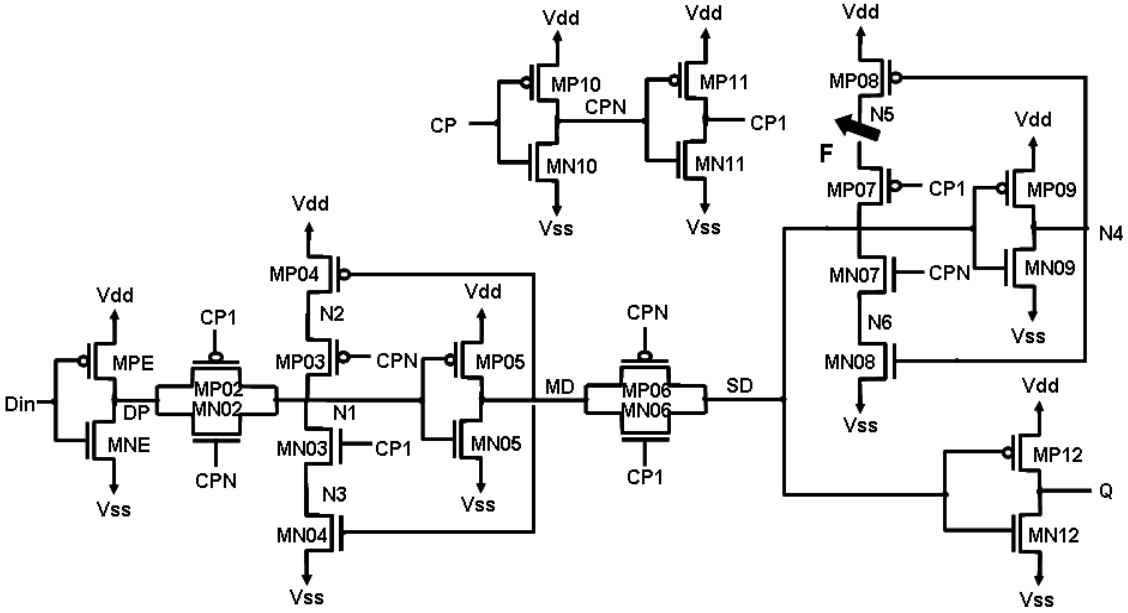


Figure 5-11: SOP on drain/source of transistor MP08

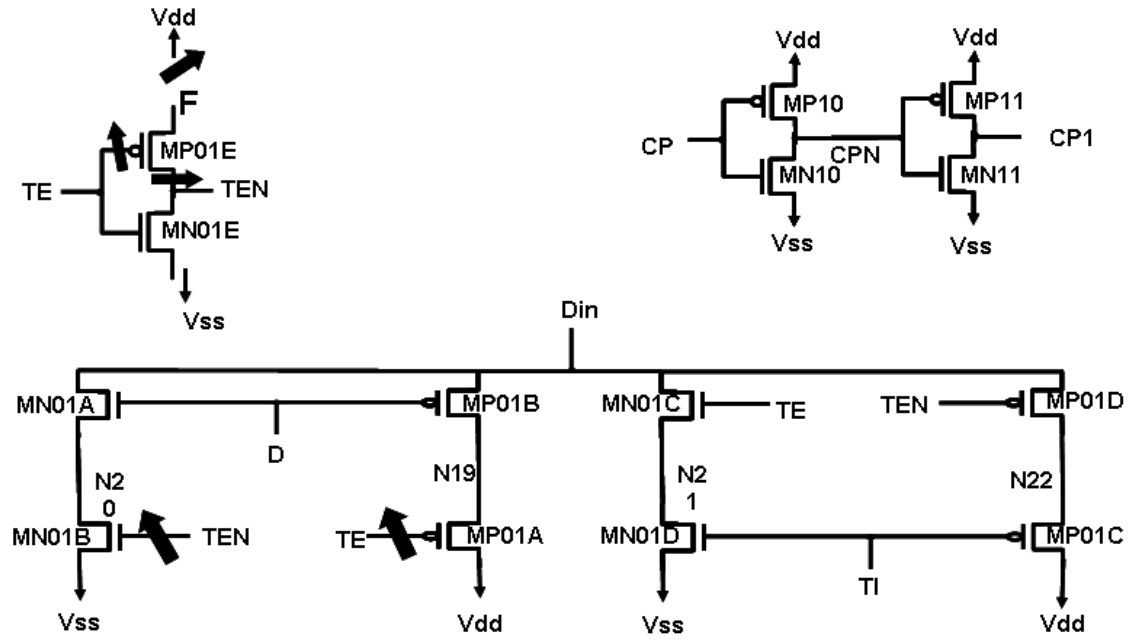


Figure 5-12: SOPs detected by ATPG test with TE = 10

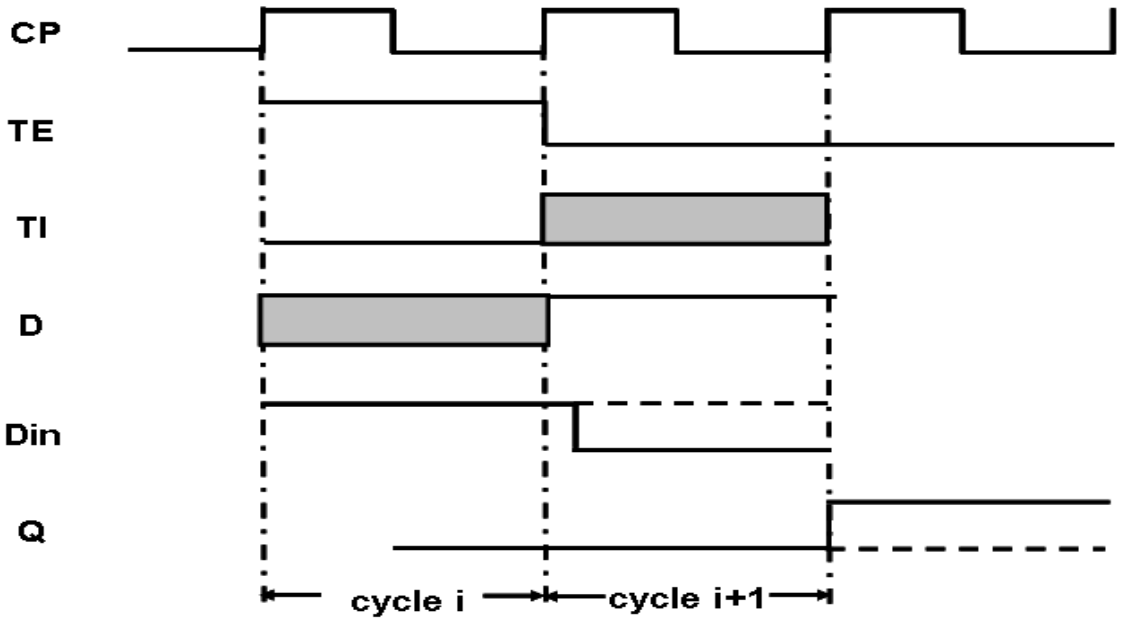


Figure 5-13: Detection of SOP on drain/source of MP01E

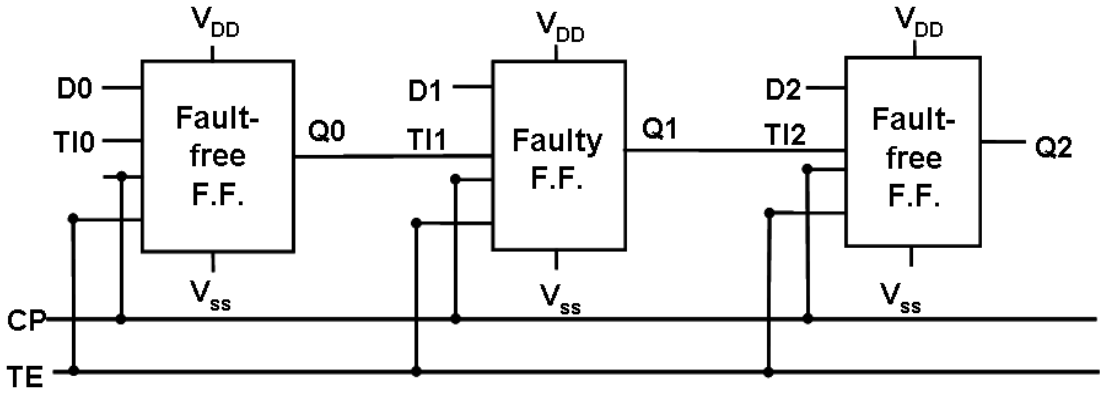


Figure 5-14: Logic diagram of a scan chain with length 3

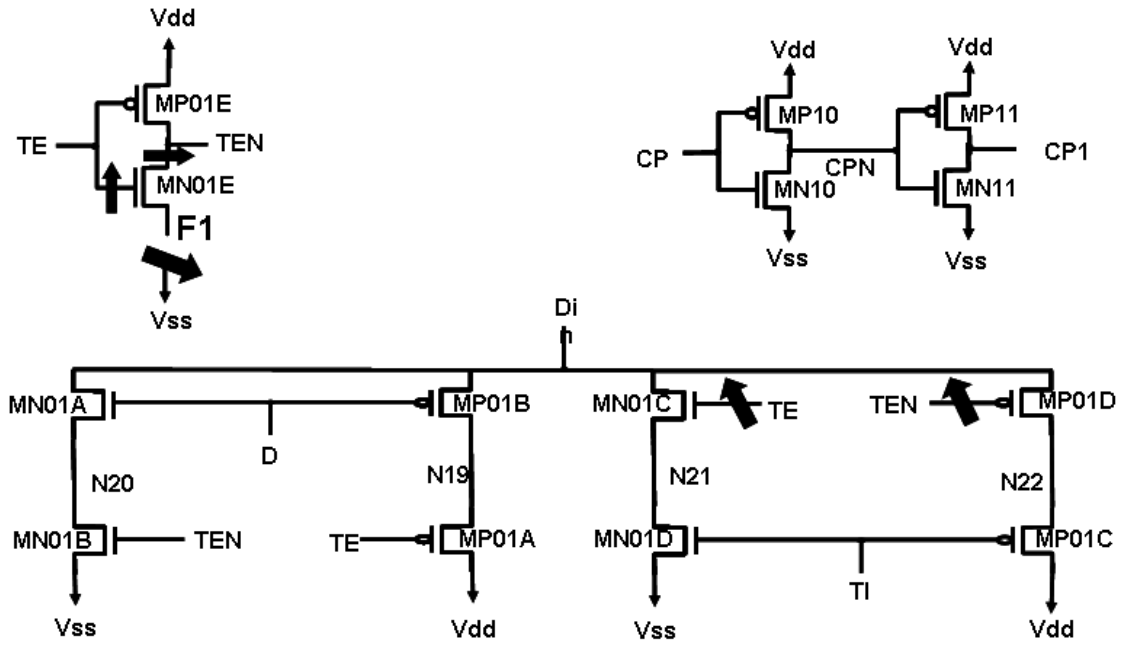


Figure 5-15: SOPs detected by ATPG test with TE = 01

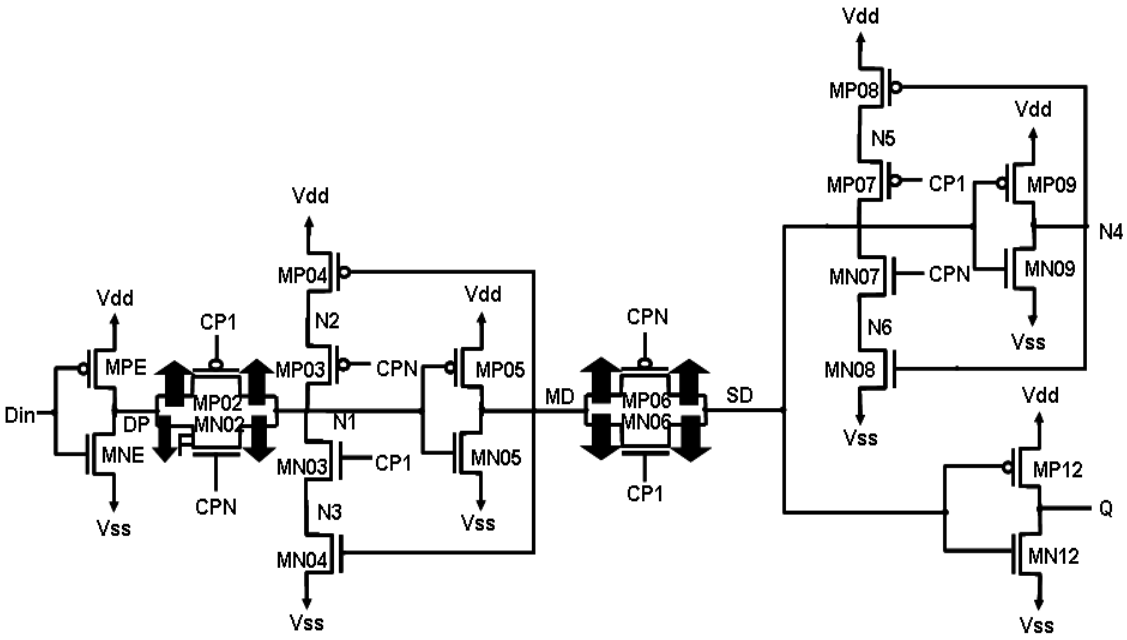


Figure 5-16: Undetected stuck-open faults

CHAPTER VI ENHANCED TESTS AND METHODS FOR DETECTION OF INTERNAL RESISTIVE OPEN FAULTS IN SCAN CHAIN

In Chapter V, it has shown that new tests are required for the detection of a large percentage of scan cell internal open faults which are not detected by the existing tests. The new tests detect all detectable large resistance opens. However, the additional coverage due to the new tests drops significantly when opens with moderate resistances are considered. In this chapter we propose to augment earlier test methods to detect internal scan chain opens with a wider range of resistances. The newly proposed method includes application of tests at higher temperatures and modifications to an earlier proposed flush test. We also present an analysis to explain the additional coverage obtained by the proposed test methods.

6.1 Introduction

Open defects frequently occur in the current VLSI technologies [6.13, 6.14] and are modeled by inserting resistances at the fault sites. In Chapter V we considered transistor large resistance opens internal to scan cells [6.2]. In [6.12] high resistance interconnect opens internal to scan cells were considered. Typically, two-pattern tests are required for the detection of SOPs [6.15]. The use of stuck-at tests [6.20] and IDDQ tests to detect complete (infinite resistance) opens have also been studied [6.16-6.18]. A new set of flush tests together with the ATPG boundary tests were shown to detect all detectable large resistance transistor opens internal to scan cells [6.2]. In [6.12], the coverage of interconnect opens by standard scan based ATPG generated tests were considered for detection and diagnosis. Since only traditional chain flush test were considered and no improved flush tests or advanced test methods were considered in [6.12], fault coverages achieved were lower than by the tests proposed in [6.2]. However,

the additional open fault coverage obtained by the tests proposed in [6.2] drops dramatically as the open resistances decrease.

In this chapter, we consider resistive open faults at the three terminals of transistors in the scan cells with lower resistance values. The value of open resistance can range from a few kilo-Ωs to tens of giga-Ωs [6.21]. We present an improved set of tests to increase the range of resistances of detected opens. We show that by replacing one of the normal-speed flush tests of [6.2] with the corresponding half-speed flush test [6.1] improves the range of open resistances detected. In addition, flush tests applied at higher temperatures are shown to significantly improve the range of open resistances detected. Theoretical analysis to explain these improvements is provided. High temperature testing adds to the test cost. However, devices with embedded DRAMs require high temperature testing [6.27]. Many designs have embedded DRAMs. Therefore, the added test cost of the proposed method will be minimal.

The remainder of the chapter is organized as follows. In Section 6.2 we review the methods for detection of resistive open fault. The tests proposed in [6.2] to detect large resistance open faults in scan cells are reviewed. We also discuss the open faults we consider and present the coverage gaps of the tests to detect resistive open faults. In Section 6.3 we present the proposed methodology and discuss the improvements in the scan cell internal open faults coverage. We also give an analysis which supports the achieved improvements. Experimental results are also shown. Section 6.4 concludes the chapter.

6.2 Preliminaries

In this section we review known methods for detection of resistive open faults. The opens in a scan cell is classified into 6 classes in this work. The opens considered in this chapter are also discussed. The tests proposed earlier for large resistance opens in

scan cells are also reviewed. In addition, the coverage gaps of the considered tests for resistive opens identified from experiments are shown.

6.2.1 Resistive open faults

A **resistive open** in which the resistance is finite appears when the conductive material is not completely broken. Contacts/vias are likely the places for resistive opens to occur [6.28, 6.29]. It implies that the faulty node F in Figure 6-1 would be charged or discharged to the expected value if a long enough time is given. The length of the charging (discharging) time depends on the value of resistance and also the threshold voltages of the driven transistors. It has been found that some resistive opens could be hard to detect due to the unknown open resistance. Since given long enough time the faulty node is going to be set to the fault-free value, the resistive stuck-open fault may lead to transition delays. This is shown in [6.30] that the length of time to charge up the faulty nodes depends on the resistance of the fault and current leakage. If the resistance is large enough such that the delay caused by the open fault is long enough to be captured, such opens can be detected by the delay tests. [6.28] investigated the resistive open detectability using delay fault testing. It shows that the process parameter variation must be taken into account to define the pass/fail limit. Therefore, delay tests can detect open faults only in a specified interval of resistance values. In order to detect larger range of resistive opens or smaller resistance opens, at-speed tests for the detection of small delay faults may be one alternative method.

In addition to the open resistance, the initial logic value at the faulty node also affects the detectable range of resistive opens. This is because the time to charge up the faulty node is longer if the fault node has the initial value which is faulty. The behaviour of a CMOS symmetrical flip-flop under resistive opens is investigated in [6.19]. The faults considered in [6.19] are high resistive opens in gates of transistors. These defects depend on initial conditions before applying tests. In addition, the dependence of the

detectability of opens on the duty cycle is also investigated. In [6.19] it showed that high resistive opens located at gates of the transistors are influenced by initial conditions prior to the application of the tests. In Chapter V, the test sequence 00…011…100…0 is suggested to charge the faulty node to the required initial value by 00…0 before activate the fault by a test bit 1 [6.2]. In [6.19] authors state that shorter duty cycles and cycle time can detect smaller values of resistive opens. This is because smaller resistive opens introduce shorter delays. In order to detect smaller delays, high frequency tests are recommended. However, this is not always true for the detection for some open faults. For some faults detection, retention tests are needed [6.31]. In this test, logic 0 or 1 is applied to each scan cell and it is observed whether the scan cell can retain the value for an "unlimited" amount of time. Hence, this test is applied at very low frequency. Besides, [6.19] only proposed tests for opens at gate in data signals. Detection of clock related control signals also need special attention.

Detecting small resistive open fault remains difficult. One to detect smaller resistive opens is to apply low or high temperatures during the testing. Since lower (higher) temperature can increase the open resistance for some materials. Hence, the smaller resistive opens can be detected at lower (higher) temperatures. In today's technology, a silicide thin film is deposited on top of the polysilicon as a shunt layer to reduce the effective resistance of the polysilicon. [6.32] described the failure mechanism of a major class of high resistance interconnects. It showed that silicide opens are caused by agglomeration which will become more sever in deep-submicron technology due to the smaller dimensions. In addition, because of the negative resistance temperature coefficient (RTC) of the polysilicon, the resistances of defective local interconnects increase with lower temperatures. Thus, the delay caused by the open defect is increased. Hence, the silicide open defect is more likely to be detected by the delay tests at lower temperatures. This technique can also be extended to improve the detectability of other defects that have negative RTC, e.g., a partial open defect at the interface between via

plug and metal. However, low temperature testing method depends on the open failure mechanism, i.e. the RTC for the material used in the defect is required to be negative. Therefore, other open defect mechanisms or defect materials need to be investigated. Moreover, keep decreasing the temperature or increasing the temperature to unrealistic level may not be doable.

In [6.33], it demonstrated how the logic testing, delay fault testing and current testing strategies can be used to detect floating gate faults in logic gates. Two important concepts are introduced to describe the detectability of the faults: 1) Predictable parameters include both technological information from the process and topological information from layout such as coupling capacitance values. 2) The unpredictable parameters include the random information coming from the size, location, and nature of the defect causing the floating gate fault. In addition, it also shows that logic (functional) test, delay fault testing and IDDQ testing only detect such fault for a given range of the unpredictable parameter. For capacitance values intervals, the detectability of those test strategies varies. Therefore, it suggests that a combination of voltage and current test strategies should be used to optimize coverage of floating gate transistor faults. [6.33] also showed many simulation data to demonstrate the detectability dependency on transistor parameters and faulty node related parameters (capacitance connected to the faulty node and resistance of open defect). However, considering those parameters into the scan cell internal fault detection is cost considerable and may not be feasible, especially for those unpredictable parameters. However, it is worth to investigate the fault coverage change and detectable resistance range of opens on those predictable parameters such as power supply voltage, internal driver strengths optimization and transistor parameters in different technologies, e.g., 90 nanometer and 65 nanometer, etc.

6.2.2 Tests and open faults considered

In Chapter V, we proposed a set of 6 scan stuck-open flush tests shown in Table 6-1 and discussed next.

The three typical flush tests, all ones (11…1), all zeros (00…0) and the 0011 sequence repeated over the length of the scan chain (0011…), are ordered as shown in the Table 6-1. Applying 11…1 helps to initialize the faulty nodes for the fault detection that needs proper initial condition. This is followed by 00…0 which generates the 1 to 0 transition necessary to detect some faults and also initializes the faulty nodes for fault detections requiring multiple cycles of TI = 0. Next, the normal-speed flush test 0011… is applied to detect additional faults. Next, the clock is held at 1 for M clock cycles to initialize the clock lines to 1. This is followed by scanning another normal-speed flush test 0011…. Next, the clock is held at 0 for N cycles to pre-charge clock lines to 0. Then, the half-speed flush test 0101… is applied. In a half-speed flush test [6.1] described in Chapter III, the flush test is applied at half the frequency at which the scan chain is closed (i.e., the shift cycle time S = 2T if the timing closure cycle time for the scan chain is T). In such a test, the TI inputs to the scan cells change during the clock = 1 phase [6.1]. This guarantees the detection of some additional open faults as shown in Chapter V. Finally, the two bit test 01 is applied at very low frequency. Note that if the higher switching activity caused by 0101… is unacceptable one can replace it with the traditional flush test 0011… [6.2].

The ATPG generated tests and the stuck-open flush tests described above, referred to as *stuck-open tests* in the sequel of this chapter, detect all detectable large resistance stuck-open faults within the scan cells. In this chapter, we consider stuck-open tests and optimize the test set to detect the scan cell internal opens with as wide a range of resistances as possible.

In Chapter V we assumed that the open has very large resistance of 100 mega-Ohms. In this chapter, our goal is to detect opens with smaller resistances. A finite

resistance is inserted between the faulty node F and the node to which it would otherwise be connected. For the faults of Figure 6-1(a), the open fault is present at the gate terminal. The initial state of the affected transistor depends on the trapped charge on node F and the transistor can either be off or on. The transistor is turned on (off) if we keep node c at 1 (0) for a long enough time. For the open of Figure 6-1(b), the effect of the resistive open in the source/drain of the transistor will be to increase the transition delay of the affected transistor. In [6.22, 6.23] it was shown that the coupling effect of the neighboring lines can help in the detection of resistive opens by means of delay testing. When the neighboring lines are set to a value opposite to the value expected on the faulty net, the delay caused by the open will increase and hence the open with smaller resistance is detected. However, such a method requires the layout information of each scan cell of the scan chain. In this work, we consider the scan cell at the transistor level and ignoring the coupling effects from the neighboring lines.

There are a total of 34 transistors in the scan cell shown in Figure 2-1 and hence we consider 102 open faults in the scan cell studied. We classify the open faults into 7 classes based on the tests described in Chapter V assuming the open resistance of 100MΩ. This classification is demonstrated in Figure 6-2 and discussed next.

From left to right in Figure 6-2, Circle 1 shows that 20 faults of class 1 (C1) are detected only by ATPG boundary SAF/TDF tests. Circle 2 shows that 12 faults of class 2 are solely detected by either the normal-speed or half-speed flush tests, which are the third and fifth flush tests in Table 6-1. Another class C3 of 28 faults is detected by both the test types. The third circle (C4) shows that 22 faults of class 4 are detected by only the slow speed flush tests. The last circle represents the faults for which detection requires proper initial conditions. Six faults in class 5 are detected by the three ordered flush tests of Table 6-1. An additional 6 faults are detected by the flush tests after pre-charging clock lines to 1 or 0. Finally, eight faults in class 7 are left undetected.

Table 6-1: Scan stuck-open flush tests proposed in Chapter V

Tests	Comments
11…1	Normal-speed flush tests in this designated order
00…0	
0011…	
Hold clock signal at 1 for M cycles	Normal-speed flush test after pre-charging clock lines to 1
0011…	
Hold clock signal at 0 for N cycles	Half-speed flush test after pre-charging clock lines to 0
Half-speed flush test 0101…	
Applying 01 slow for 2 cycles	Slow speed flush test

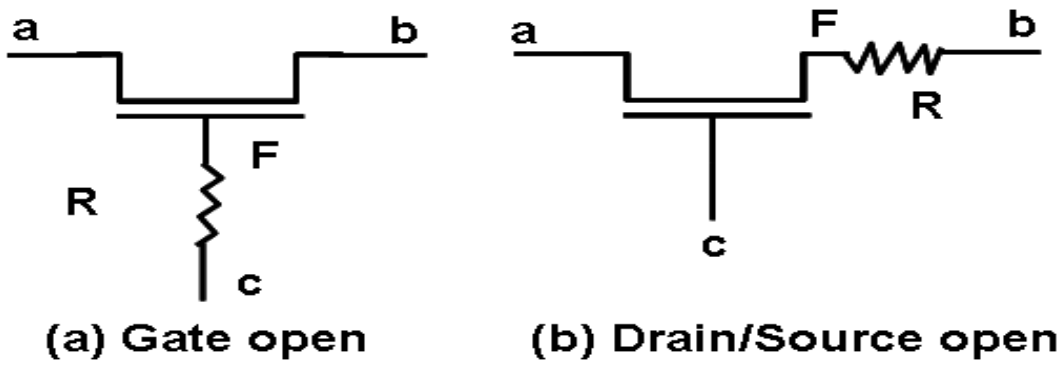


Figure 6-1: Resistive stuck-open fault model

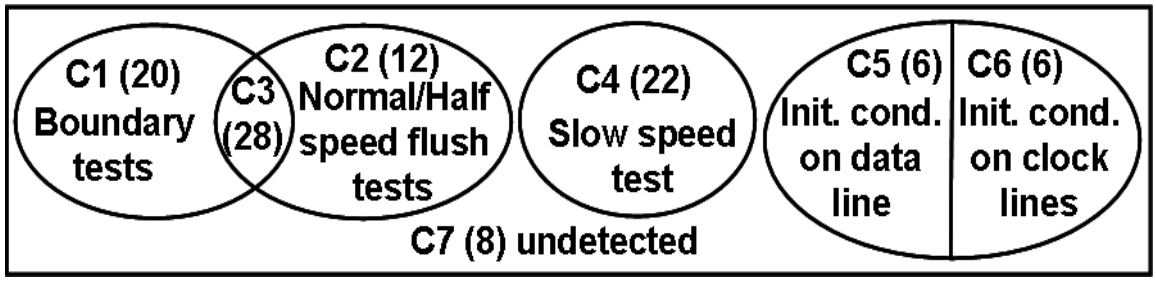


Figure 6-2: Classification of transistor open faults

6.2.3 Coverage gaps of scan stuck-open tests for resistive opens internal to scan cell

We observed as the resistance decreases, the fault coverage of the stuck-open tests described in Section 6.2.2 drops significantly. Table 6-2 shows the simulation results at a temperature of 25 centigrade (℃) for the open faults if the open resistances are 100MΩ, 4MΩ, 400KΩ and 40KΩ which are representatives for large, medium and small resistances. The fault coverages are reduced by 33.4%, 47.1% and 91.2% if the open resistance drops from 100MΩ to 4MΩ, to 400KΩ and to 40KΩ, respectively. Therefore, a cost-effective method to detect smaller resistance opens is necessary.

Table 6-2: Fault coverage of the stuck-open tests to detect resistive opens at 25℃

Open Resistance	100MΩ	4MΩ	400KΩ	40KΩ
Fault Coverage	92.2%	58.8%	45.1%	0.98%

6.3 Proposed methods to improve fault coverage of resistive open faults

In order to detect scan cell internal open faults with wider resistance range, we propose to modify the stuck-open tests described in Table 6-1 by replacing the fourth normal-speed flush test 00110011… with a half-speed flush test 00110011… as shown in Table 6-3. Note that, as with the flush tests of Table 6-1, if the higher switching activity caused by 0101… is unacceptable, the fifth and the sixth flush tests can be replaced by 00110011… and the 5-bits test 00110, respectively. We also propose applying tests at higher temperatures to further improve the fault coverage when the open resistances are small.

Before discussing the motivation for these changes, we present results to demonstrate their effects. We performed HSPICE simulations using a segment of a scan chain with three scan cells as shown in Figure 6-3. The targeted open fault with an inserted resistance was injected into the second flip-flop. The tests in Table 6-3 together with the ATPG TDF tests targeting D and Q were applied with the ambient temperatures of 25℃ and 125℃. Note that the TDF tests are applied at the frequency of 1GHz and assumed 20% slack (0.2ns) for the path in combinational logic is selected. For the industrial design used in this work, the scan chain timing closure was at scan shift cycle time of 10 nanoseconds. Thus, the half-speed flush test was applied at shift cycle time of 20 nanoseconds. Holding clock at 1 or 0 for 150 nanoseconds was found to be enough to pre-charge the clock lines. The slow speed two-bit flush test is applied at shift cycle time of 1 micro-second.

Table 6-4 summarizes the simulation results. Rows 2 and 3 show the fault coverages for the open resistances of 100MΩ, 4MΩ, 400KΩ and 40KΩ, respectively. In the following subsections, we present explanations for the coverage improvements discussed above. We also discuss the observation that the ATPG TDF tests have better performance than the flush tests in detecting some open faults with smaller resistances. Comparing the results in row 2 of Table 6-4 to Table 6-2, the fault coverage at 25℃ is increased by about 3% for the open resistances of 4MΩ, 400KΩ and 40KΩ. Therefore, the new tests detect 3% more open faults than by the tests described in Table 6-1 [6.2] at 25℃. We will analyze this improvement in Section 6.3.2. By increasing the temperature at which the testing is done to 125℃, the coverage is enhanced by over 22% for the open resistance of 4MΩ. We observed that the majority of this coverage enhancement is contributed from the faults in class 4 (cf. Figure 6-2). We will discuss this further in Section 6.3.1. The faults detected over and above those detected by the tests in Table 6-1 when resistances are 400KΩ and below are all in classes 1 and 3 (cf. Figure 6-2). The faults in these classes are detected by either ATPG boundary tests or both by the ATPG

boundary tests and flush tests. For the data reported in Table 6-4 we used the results for ATPG boundary TDF tests. We discuss this further in Section 6.3.3.

Table 6-3: *Scan resistive stuck-open flush tests* proposed

Tests	Comments
11…1	Normal-speed flush tests in this designated order
00…0	
0011 …	
Hold clock signal at 1 for M cycles	Half-speed flush test after pre-charging clock lines to 1 (this is the modified test)
0011 …	
Hold clock signal at 0 for N cycles	Half-speed flush test after pre-charging clock lines to 0
Half-speed flush test 0101…	
Applying 01 slow for 2 cycles	Slow speed flush test

Table 6-4: Fault coverage by applying the proposed tests at higher temperatures

Open Resistance	100MΩ	4MΩ	400KΩ	40KΩ
25℃	92.2%	61.7%	48.0%	3.9%
125℃	92.2%	84.3%	48.0%	5.9%

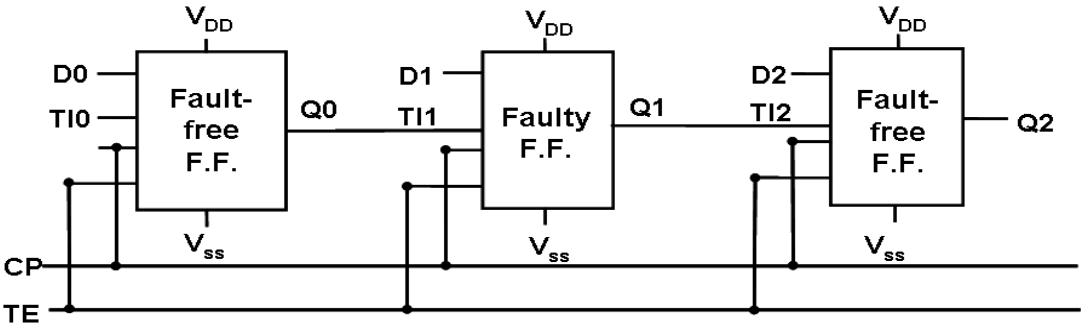


Figure 6-3: Logic diagram of a scan chain with length 3

6.3.1 Leakage current effects on the detection of faults in class 4

Leakage current is becoming significant due to the shrinking sizes of transistors. Besides, leakage currents increase with increase in ambient temperature [6.24]. The faults of class 4 are located in the part of the scan cell used to retain the logic value from the previous clock phase. This class of faults can only be detected by the slow speed flush tests. The detection of these faults depends heavily on the leakage currents. We found that the increased leakage currents due to higher testing temperature prevent the expected value from being retained on the scan cell internal nodes. This will widen the detectable resistance range of this class of internal opens.

As an example, consider the open fault at the drain of transistor MP03 highlighted by an "X" in Figure 6-4. The faulty transistor is in the branch of the circuit used to retain the value at node N1 from the previous half clock cycle. This fault is detected by the slow-speed flush test described in Table 6-3. When CP = 0, a logic value 1 enters the master latch at node N1 since transistors MP02 and MN02 are on. The node MD is then set to 0 and hence MP04 is turned on. When CP switches to 1, MP03 is turned on since CPN = 0. The node N1 is thus driven by Vdd through the transistors MP04 and MP03 and the logic value 0 at MD propagates into the slave latch in the fault-free circuit. However, in the faulty circuit the node N1 is floating due to the open in MP03. If we apply the test slow enough to let N1 discharge towards 0, this will turn on MP05 and turn off MN05. The faulty value 1 at MD is then generated and propagated to the output Q. Note that the detection of this fault also requires the open resistance to be large enough such that the current charging the node is smaller than the discharging current at N1.

At node N1, five possible currents will be present when CP switches to 1 as illustrated in Figure 6-4. I_1 is the current charging the node N1 from Vdd through MP04 and the faulty transistor MP03. The larger the open resistance is, the smaller the value of I_1 will be.

When CP = 1, both MN02 and MP02 are off. I_2 is the subthreshold leakage current between sources and drains of MN02 and MP02. Note that this leakage current is present only when the nodes DP and N1 have different values during the phase where CP = 1 (i.e., TI is required to change when CP = 1). I_3 and I_4 are from the combination of parasitic leakage current through gate-to-source/drain extension overlap region and gate to inverted channel current [6.24]. Since N1 holds the value 1, the majority of gate leakage goes to Vss and the node MD through MN05 and MP05, respectively. Since MD = 0 when CP = 1 as the initial state in the faulty circuit, MN04 is turned off and MN03 is on. Similar to I_2, I_5 is the subthreshold leakage current from N1 to Vss through MN03 and MN04.

According to the detection condition described earlier, increasing the discharging currents ($I_2 + I_3 + I_4 + I_5$) or decreasing the charging current I_1 can detect the open fault with smaller resistance. One way to accomplish this is to raise the testing temperature. The subthreshold leakages I_2 and I_5 can be expressed as follow [6.25]:

$$I_{sub} = \mu_0 C_{ox} \frac{W}{L} (m - 1)(V_T)^2 e^{(Vg - Vth)/mV_T} (1 - e^{-V_{DS}/V_T}) \quad \textbf{(1)}$$

where μ_0 is the effective mobility, C_{ox} is the gate oxide capacitance, W/L is aspect ratio of the transistor, m is the body effect coefficient, V_T is the thermal voltage and V_{th} is the threshold voltage. Vg and V_{DS} are the gate and drain-source voltages, respectively. By raising the temperature, V_{th} decreases and V_T increases linearly. Thus, I_2 and I_5 exponentially increase as the testing temperature is raised.

The contact and via resistance is a function of temperature as follows:

$$R(T) = R_0 [1 + C_1(\delta T) + C_2(\delta T)^2] \quad \textbf{(2)}$$

where $\delta T = T - 25^{\circ}C$. C1 and C2 are the parameters for different types of vias. Thus, I_1 will decrease due to the increased open resistance during elevated temperature slow speed test. I_3 and I_4 are weakly dependent on the temperature [6.26]. Therefore, the increased I_2 and I_5 and the decreased I_1 due to the higher temperature prevent the node N1 from

retaining the fault-free value 1. Hence, applying the slow speed flush test at higher temperature will detect the open fault shown in Figure 6-4 with smaller resistance.

Note that replacing the low frequency test 01 with 11 also detects this fault. However, since I_2 will not be present in the latter case the detectable resistance range of the open will be narrower.

To determine the enhancement of the detectable open resistance range by raising the testing temperature, we performed simulations on the fault discussed above at different temperatures and determined the smallest detectable resistance (Rc) of the fault. The simulation results are shown in Table 6-5. If the temperature increases from 25℃ to 125℃, the smallest detectable resistance is reduced by 88.2%.

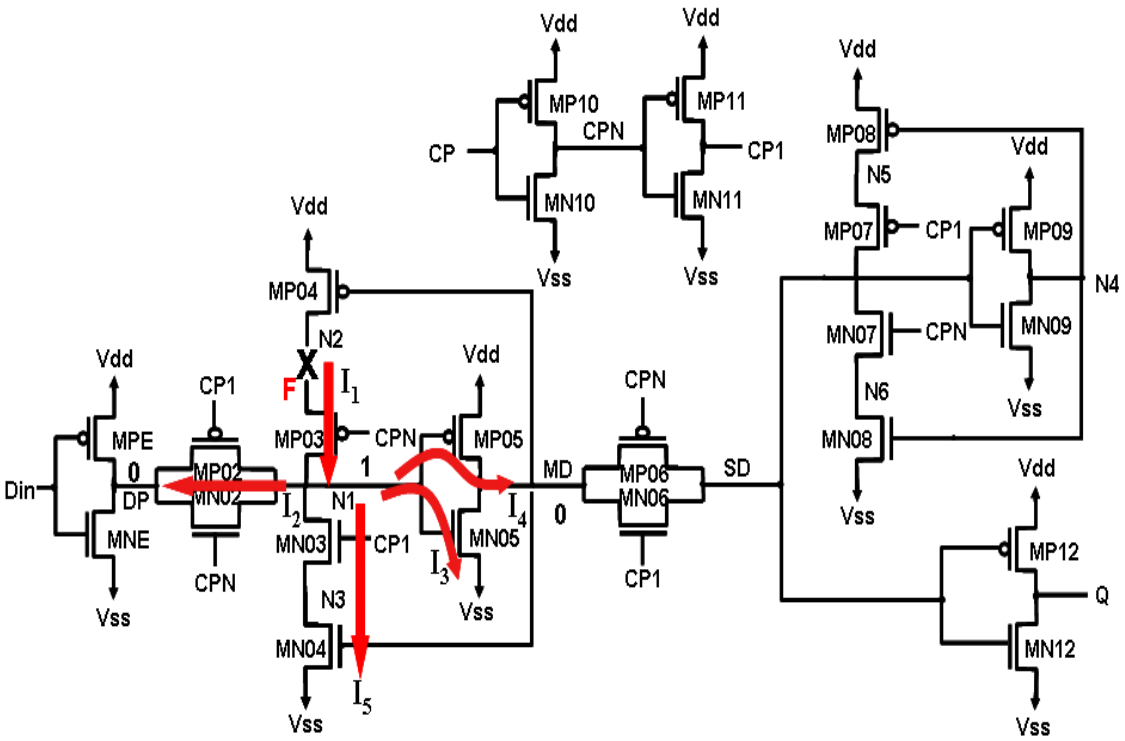


Figure 6-4: SOP on drain/source of transistor MP03

Table 6-5: Simulation results for MP03 drain open at 25℃, 50℃, 75℃, 100℃ and 125℃

Temperature	25℃	50℃	75℃	100℃	125℃
Rc	17MΩ	8MΩ	4MΩ	3MΩ	2MΩ

6.3.2 Widening detectable resistance range of faults in class 6 by slower speed flush tests

Typically, resistive open faults can be detected by delay tests targeting small delay defects [6.19]. The faster the test is applied, the smaller the resistance of detected opens. However, we found that the slower speed test can detect some faults in class 6 with smaller resistances. This class of faults may be detected by both the normal-speed flush test and the half-speed flush test after pre-charging clock lines to 1. However, we observed that opens with smaller resistances are detected by the half-speed flush test at 25℃. The 3% coverage improvements are due to this class of faults detected by the half-speed flush test of Table 6-3 that replaced the normal-speed flush test of Table 6-1. Next, we discuss detection of one of these faults.

Consider a class 6 open fault located on the gate of MN06 shown in Figure 6-5. The fault site is highlighted by an arrow and F denotes the faulty node. In the fault-free circuit, the node F is connected to CP1. The detection of this fault requires holding the clock at 1 to charge F to 1 before applying the flush test. We refer to Figure 6-5 and Figure 6-6 in the following discussions. Note that in the normal speed flush test TI can change value either when CP = 0 or CP = 1 depending on the path delay between TI and the output of the previous scan cell. Assume that the shift mode of the scan chain has been closed during timing closure for 1/T Hertz (i.e., the maximum delay between the scan cells in the scan chain is T). Figure 6-6(a) shows the waveforms of CP, TI, CP1, F and Q when TI changes value in the CP = 0 phase in the normal-speed flush test applied

with the clock cycle S = T. When CP = 0 in cycle i, CP1 is 0 and MN06 is turned off in the fault-free circuit. The changes of TI will not propagate to the output Q. However, in the faulty circuit F is initialized to 1 and discharges slowly which strongly depends on the open resistance. Hence, MN06 is turned on when CP = 0. The change of TI from 1 to 0 in cycle i will propagate into the slave latch and to the output Q. The faulty value Q = 0 is then observed at the next rising edge as shown in Figure 6-6(a). Similarly, this fault is also detected by applying the half-speed flush test with the shift cycle time S = 2T which guarantees that the changes of TI happen when CP = 1 as shown in Figure 6-6(b). In the faulty circuit, Q in Figure 6-6(b) changes at the falling edge of the cycle i whereas it changes at the time TI changes in Figure 6-6(a). Therefore, both the normal speed flush test and the half-speed flush test may detect this fault if the open resistance is large enough.

Fault detection requires the change of TI to propagate through the affected transistor MN06 before the node F discharges down to turn off MN06 as shown in Figure 6-6. However, we cannot control the change of TI directly. The timing of the change of TI depends on the path delay (dp) between TI and the output of the previous scan cell in the scan chain. Since F starts discharging in the CP = 0 phase and charging when CP = 1, in the case of changing TI when CP = 0 the fault is detectable only if the delay (d) caused by the open fault is greater than (dp – S/2) as shown in Figure 6-6(a). However, in the case shown in Figure 6-6(b) the TI transition always happens before F starts to discharge. Therefore, the half-speed flush test detects smaller resistance faults.

We simulated the flush tests in Table 6-1 and Table 6-3 for this fault to determine the detectable resistance range enhancement by the newly proposed flush tests. Table 6-6 shows that by applying the half-speed flush test after pre-charging clock lines to 1 the smallest detectable resistances are reduced by 97.8% and 97.2% at temperatures 25℃ and 125℃, respectively.

Table 6-6: Applying the tests in Table 6-1 and Table 6-3 to MN06 drain open fault

Tests	25℃	50℃	75℃	100℃	125℃
Old tests [6.2]	6.6MΩ	6MΩ	5.6MΩ	5.3MΩ	5.1MΩ
New tests	145KΩ	143KΩ	143KΩ	142KΩ	142KΩ

6.3.3 Observation on ATPG boundary TDF tests vs. flush tests in detecting faults in class 3

The ATPG TDF tests are applied at a speed much faster than the normal flush tests. Faults in class 3 (cf. Figure 6-2) are detected by both the flush tests and the ATPG TDF tests. However, we found that the ATPG boundary TDF tests can take advantage of the delay from the combinational logic for the detection of smaller resistance opens in this class.

Consider a fault in this class, the drain open in MNE highlighted by an arrow in Figure 6-7. The node Din, the inverse of the scan cell input, gets the value from the multiplexer shown in Figure 2-1. To detect the fault, we should first initialize the node DP to 1 by setting Din = 0 since MPE is on. In the second pattern, we need to set Din to 1 which turns on MNE in the fault-free circuit. Hence, DP will be set to 0. However, in the faulty circuit DP retains the value 1 due to the open fault at the drain of MNE. This is shown in Figure 6-8 where the output Q retains the value 1 in cycle i+2. The detection condition of this fault is TE = 11, TI = 10, D = XX or TE = 00, TI = XX, D = 10 where X denotes a do not care. Therefore, both the normal-speed flush test 0011…and the ATPG test targeting D slow-to-fall fault detect the fault.

The delay (dr in Figure 6-8) caused by the open fault is dependent on the value of the open resistance. The detection of the fault requires that (dp + dr) will be greater than one full cycle time S, where dp is the path delay from the output of the previous scan cell

to TI when flush test is applied or the delay from combinational logic when the boundary TDF test is applied. Since in the TDF tests cycle time S is about two orders of magnitude less than the one for the flush test, the requirement on the magnitude of dr in detecting the drain open fault in MNE by applying the TDF test is smaller. Thus, the TDF test can detect this class of faults with smaller resistance.

Table 6-7 shows the simualtion results for the fault described above tested at 25℃ and 125℃. The ATPG boundary TDF tests are applied at the frequency 1GHz (S = 1ns). The smallest detectable resistances assuming 100%, 90%, 75%, 50%, 25%, and 10% slacks for the path in the combinational logic selected by the TDF tests are shown in columns 2-7 of Table 6-7. The ATPG TDF tests take advantage of the delay through the combinational logic and can potentially reduce the detectable resistance by 91.2%. Note that by simulating the flush tests in Table 6-3 the smallest detectable resistances at 25℃ and 125℃ are 543KΩ and 463KΩ, respectively. Therefore, compared to the normal-speed flush tests the ATPG boundary TDF tests reduce the detectable resistance by over 68%.

The results reported in the last two columns of Table 6-4 are for the case of 25% slack for the combinational logic path used in the TDF tests to detect the targeted faults.

6.4 Conclusions

In this chapter we investigated the detectability of resistive opens in transistors internal to scan cells. The increased leakage currents due to raised temperature during testing can reduce the detectable resistance by up to 88%. In addition, we found that slower speed flush tests can reduce the smallest detectable resistance of a class of open faults by over 97%. Based on these observations, a new scan stuck-open flush test was proposed to detect wider resistance range of opens inside the scan cells. The proposed methodology improves the resistive open fault coverage significantly. Finally, we observed that the ATPG boundary TDF tests detect smaller resistance opens than the

flush tests for a class of faults by taking advantage of the delays in the combinational logic.

Table 6-7: Appling ATPG TDF test at 1GHz to the fault in class 3 for variable slacks of combinational logic

Temperature	100%	90%	75%	50%	25%	10%
25℃	171KΩ	164KΩ	147KΩ	104KΩ	44KΩ	16KΩ
125℃	147KΩ	143KΩ	130KΩ	93KΩ	40KΩ	15KΩ

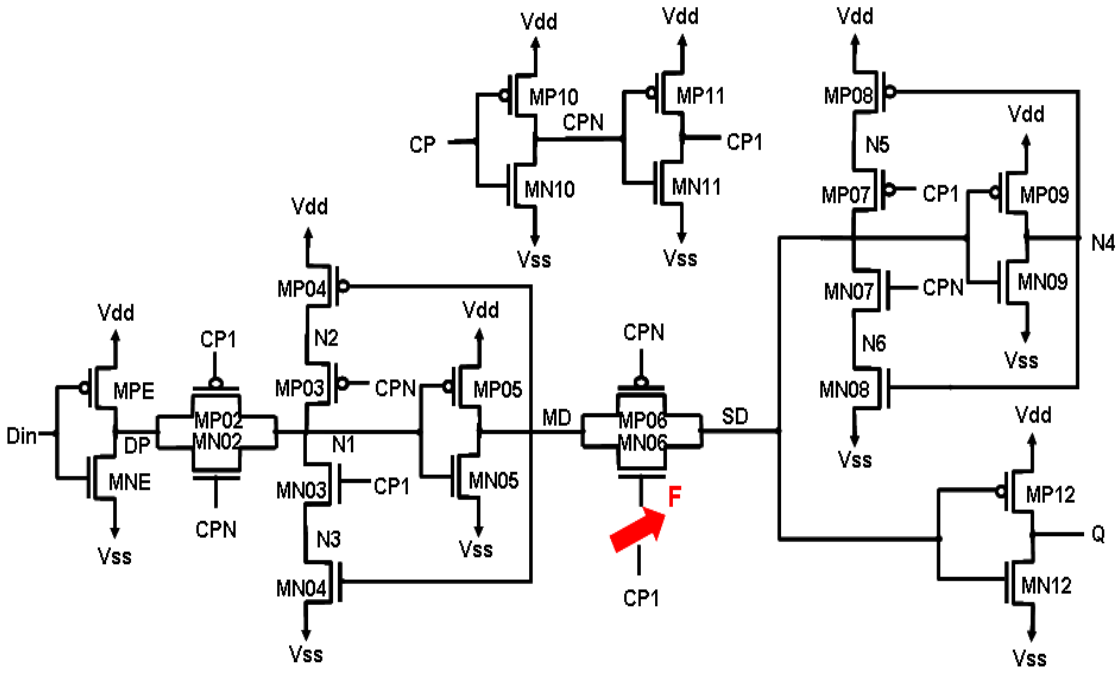


Figure 6-5: Gate of transistor MN06 stuck-open

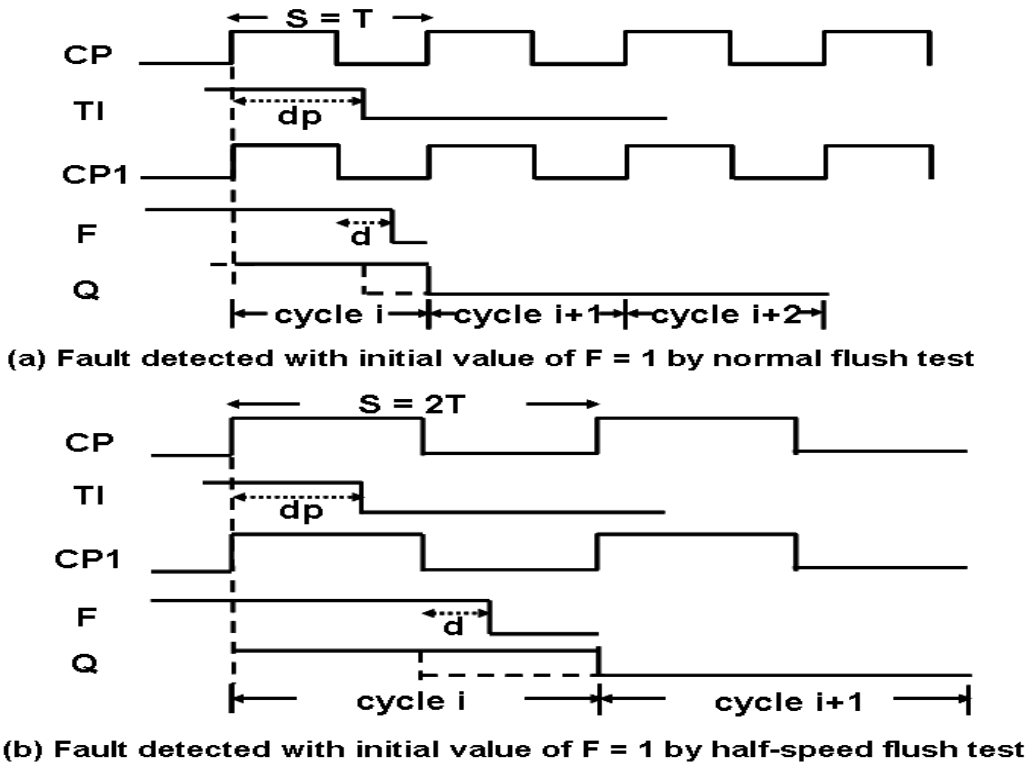


Figure 6-6: Detection of transistor MN06 gate SOP

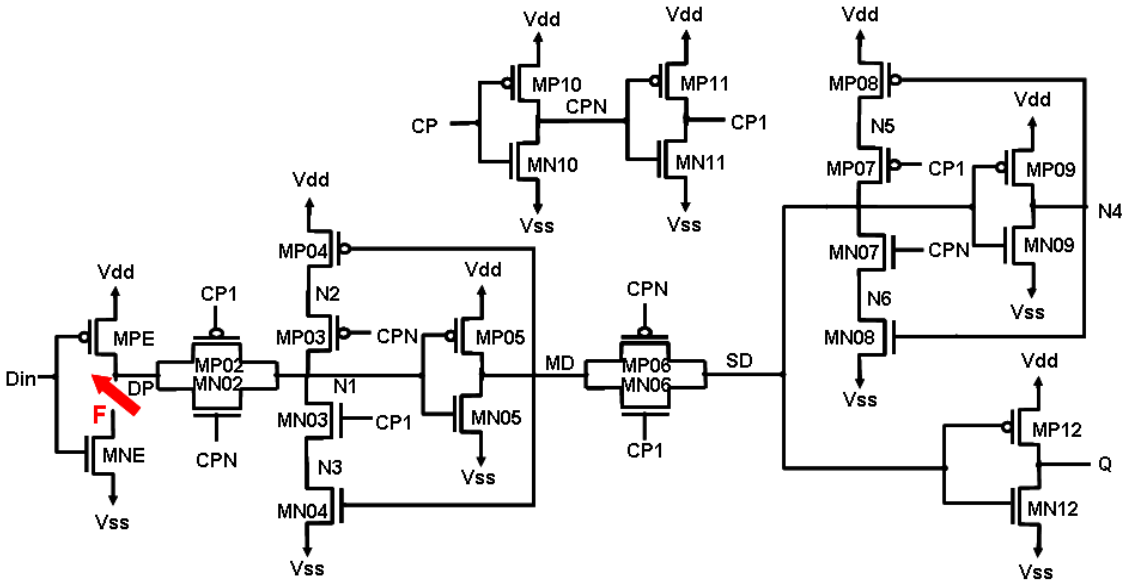


Figure 6-7: Drain of transistor MNE stuck-open

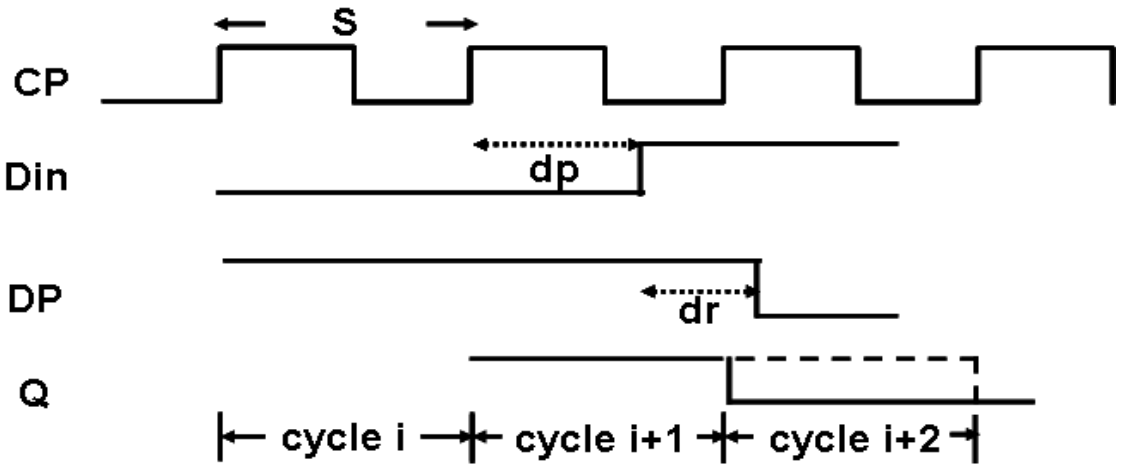


Figure 6-8: Detection of transistor MNE drain SOP

CHAPTER VII AN ENHANCED LOGIC BIST ARCHITECTURE FOR ONLINE TESTING USING SCAN STUCK-OPEN FLUSH TESTS

The objective of using Logic Built-in Self-Test (BIST) for online and periodic testing is to identify defects, like opens, resulting from the wear and tear of the circuit. We have shown that existing test sets have a low coverage for open defects located in scan flip-flops, even though such defects may affect functional operation. Existing Logic BIST structures suffer from the same limitations. As shown in Chapter V and IV, a new set of tests is proposed to detect all detectable open faults internal to scan cells. In this chapter, a novel Logic BIST architecture to detect such defects is proposed. Unlike other sequences, like checking experiments, the enhancements are simple and independent of the circuit under test.

7.1 Introduction

Logic BIST is often used in periodic system testing. The objective of these tests is to uncover defects that could occur due to the wear and tear of the circuit. Open defects are one such class of defects. We investigate the detection of open defects, specifically ones that occur inside scan flip-flops, using logic BIST.

In Section 7.2, we discuss the various BIST architectures to which this work is applicable. We also describe the results of an earlier analysis shown in Chapter V that showed the following: (1) Assuming that the set of patterns applied has 100% stuck-at and transition fault coverage, only 55.87% of the stuck-open faults in the scan chain are detected. A similar conclusion is applicable to conventional Logic BIST. (2) The faults that are not detected, if present, can cause the circuit to fail in the functional mode. Many of these faults will be hard to diagnose since they will cause intermittent failures. In addition, these failures become more important when power saving methods like clock-gating is used. (3) We review a new sequence of tests that detects these undetected faults and increases the stuck-open fault coverage to approximately 92%. The remaining 8% of

faults are on transmission gates within the scan cell which are not detectable. Based on this enhanced coverage we argue that such tests can be applied as part of the logic BIST pattern set.

In Section 7.3 we propose an enhanced logic BIST architecture that accomplishes this. Note that in [7.3, 7.4] checking experiments were proposed to detect such faults. However, the checking experiments are very long which adversely affects the test time. Such tests are also a function of the circuit under test. This becomes a barrier to an easy implementation in logic BIST. In our case we show that the test patterns are independent of the circuit under test and are amenable to a very simple BIST implementation. Finally we conclude in Section 7.4.

7.2 Preliminaries

In this section we give a brief introduction of BIST architectures and tests applied by Logic BIST. In addition, the enhanced set of tests discussed in Chapter V and VI is reviewed.

7.2.1 BIST architectures and tests applied by Logic BIST

There are two classes of BIST architectures [7.13] (i) In-situ or test-per-clock; and (ii) Scan-BIST or test-per-scan.

For in-situ BIST, a pseudo-random pattern generator (PRPG) drives all the inputs of the circuit-under-test (CUT), and the PRPG changes state once per clock cycle. A number of different variants of this are possible. Among them are built-in logic block observer BILBO [7.14] and circular self-test path (CSTP) [7.15]. State elements, like D Flip-Flops, are modified as shown in Figure 7-1(b), (c). In Figure 7-1, y_i are the inputs of the CUT and Y_i are the outputs of the CUT. For BILBO, the values of the control variables B_0, B_1 determine the mode of the state elements viz. functional, scan shift, pattern generation or response compressions.

For CSTP, the values of the control variables B_0, B_1 determine the mode of the state elements viz. functional, scan shift or response compression. In both cases, the scan shift operation is applied primarily to initialize the content of the PRPG and shift out the compressed signature.

For test-per-scan, for each clock cycle the PRPG makes a state transition and single bits are shifted into multiple scan chains driven by the PRPG. After a sufficient number of clock cycles has been applied to fill the scan chains the test is applied to the CUT. One realization of this method is the STUMPS (Self-Test Using an MISR and Parallel Shift Register Sequence Generator) architecture [7.16] shown in Figure 7-1(d). Optionally, in the STUMPS architecture, the scan-out pins can be fed into an XOR-tree to reduce the number of inputs going into the multiple input signature register (MISR). Inclusion of this XOR-tree does not change the results in any way. For simplicity, we ignore it in this discussion. The state elements are modified to enable the scan shift operation. Mux-Scan, an example of such a modification, is shown in Figure 7-1(a).

We study in detail the Mux-Scan element in the context of test-per-scan BIST. All the state elements of Figure 7-1 have D-flip-flops. The results obtained are valid, with minor modifications, for the BILBO and CSTP approaches.

For the logic BIST architecture assumed, a large number of random patterns are scanned into the scan chains and applied to the combinational circuit under test. For stuck-at faults only single cycle tests are applied. For transition faults, tests with two or more cycles are applied. We henceforth assume that logic BIST applies two pattern tests to the circuit under test (CUT).

In the context of scan testing, a set of tests called flush tests are also applied. Assume that the shift mode operation of the scan chain has been timing closed for a shift clock with time period T. Then all the shifts of scan chains to apply tests and observe test responses are done, both in logic BIST and traditional scan based external test, using a clock of period T. The waveforms of the clock (CP) and scan_in (TI) signals in Figure 7-

2 show the application of the flush test 00110011… followed by 00…0. The tests are applied to the scan chain at shift cycle time S equal to T. While the second test is shifted in, the values stored in the scan cells are shifted out and compared with the expected value. Shifting continues for K additional clock cycles, where K is the length of the scan chains.

In [7.12], we showed that many SOPs are not detected by the standard test suites that include flush tests 00...0, 11...1 and 00110011... and scan cell boundary tests for SAFs and TDFs.

In the context of Logic BIST flush tests are not explicitly applied. However, flush tests are an implicit part of logic BIST tests when random patterns are shifted in to fill the scan chain. If there is a scan chain fault, detectable by a flush test, it will corrupt the vector applied by logic BIST to the CUT. Consequently, the response of the CUT to the corrupted pattern is likely to be faulty, and this will be detected through the MISR.

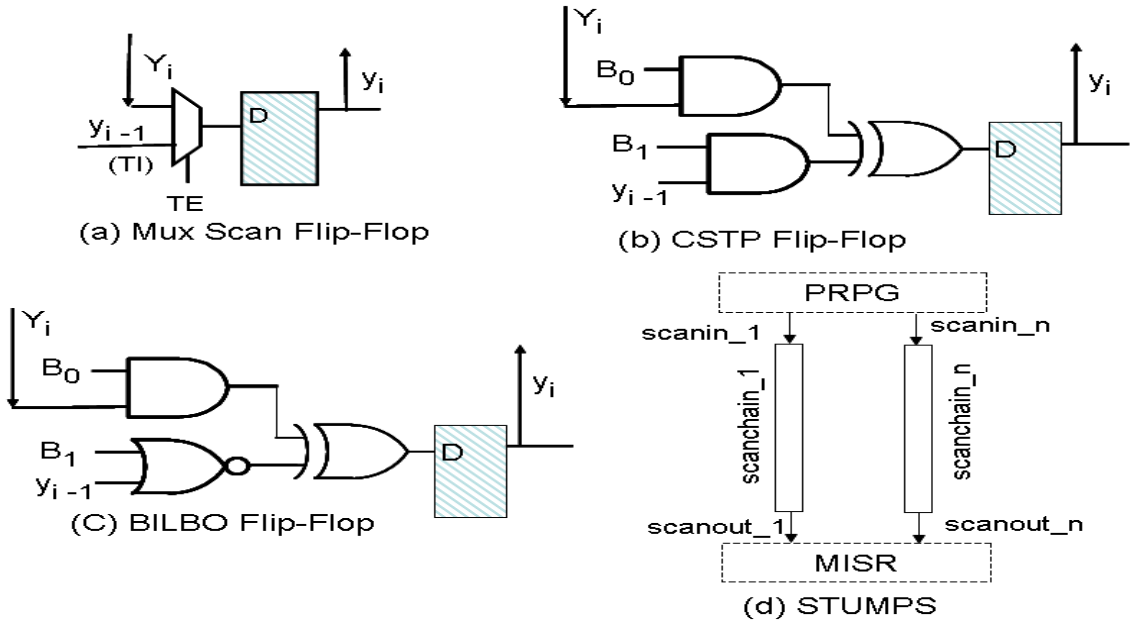


Figure 7-1: Logic BIST Structures

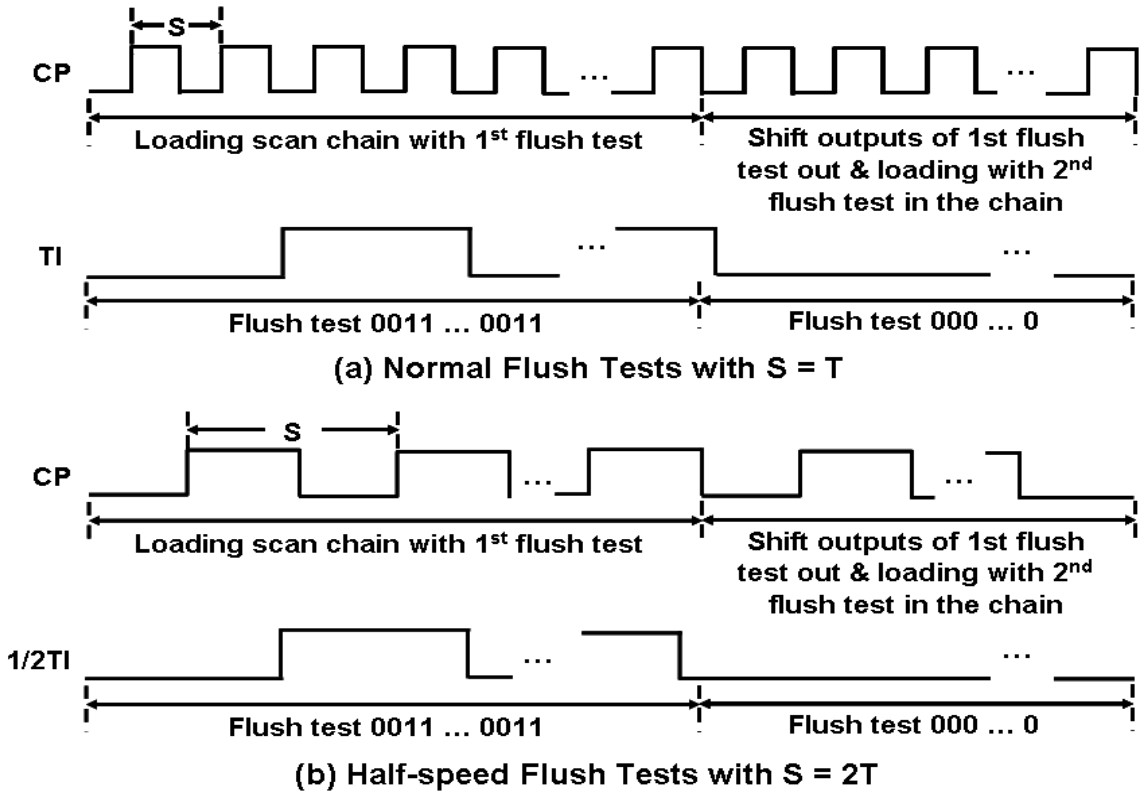


Figure 7-2: Scan testing with flush test 00110011…

7.2.2 Tests for scan cell internal open faults

In Chapter V, we proposed additional scan based tests to cover the scan cell internal faults. These studies were done in the context of manufacturing test applied through an external tester. The need to generate and apply the additional scan based tests in logic BIST, and methods to achieve this goal, are the focus of this chapter. For the sake of completeness and motivation for the work in this chapter, we include a summary of the work reported in [7.12] that considered high resistance opens in the transistors internal to scan cells. This will point out issues that have to be addressed when enhancing the logic BIST schemes to detect opens.

In Chapter V we showed that by using an enhanced set of scan based tests it is possible to increase the coverage of SOPs such that all detectable large resistance open

faults in the scan cell shown in Figure 2-1 are detected. Based on analysis of such opens with moderate resistances [7.19] described in Chapter VI, an improved set of flush tests is proposed. The sets of tests for open faults internal to scan cells are shown in Table 7-1 and Table 7-2 and are briefly reviewed below.

The tests in Table 7-1 are flush tests. The important new requirements of these tests are (1) the order of application of the tests, (2) the requirements on the period of the shift clock, and (3) holding of the scan clock at 0 and at 1 for a period of several clock cycles. The first three tests in Table 7-1 are the standard flush tests but must be applied in the order given rather in an arbitrary order as typically done in standard test suites. After the application of the three flush tests the shift clock should be held at logic 1 for duration of M clock cycles. M is the number of clock cycles required to pre-charge clock node to 1. This is done to insure charging of the clock lines of the scan cells to 1 even in the presence of high resistance open. Next, the flush test 00110011... is applied again and the clock is held at 0 for a duration of N clock cycles. N is the number of clock cycles required to charge clock node to 0. This is followed by a new flush test 0101...01 applied with scan shift clock period which is at least twice the clock period determined by the timing closure of the scan chains.

The half-speed flush tests were first introduced in Chapter III [7.5]. A timing diagram for half-speed flush tests is shown in Figure 7-2(b). If we assume that scan chain timing was closed for time period T then the half-speed flush test clock should have time period 2T. Such tests were shown to be required to detect some stuck-at and stuck-on faults in [7.5] and to detect some transistor opens in [7.12]. Finally a two bit flush test 01 is applied at much lower frequency.

For the 90 nanometer design shown in Table 1-1 the timing closure clock period for the scan chains was determined to be 10 nanoseconds. Thus the half-speed flush tests are applied at a clock period of 20 nanoseconds. A duration of 15 clock cycles over which the clock is held at 1 and 0 as described above was found to be sufficient to pre-

charge the clock nodes to 0, 1. So, N = 15 in Table 7-1. A 1 microsecond clock period for the final two bit flush test was determined to be sufficient. This last flush test is needed to test for data retention faults in the scan cells.

The additional tests shown in Table 7-2 were also found to be needed to detect some scan cell internal SOPs [7.12]. These tests are two pattern tests and target stuck-open faults on transistors driven by the test enable input TE. In normal two pattern test application using broadside test method the test enable line is held at 0 during the initialization and capture cycles. The tests in Table 7-2 require a state transition on TE during test. More importantly two of the tests require a 0 to 1 transition on TE. Such two pattern tests are not used with either broadside or skewed-load methods.

In summary, the results in Chapter V [7.12] for externally applied manufacturing tests to detect scan cell internal faults that require non-traditional tests imply that one needs to enhance patterns applied using logic BIST. This will require modification to the pattern generators and clock wave form generators used in logic BIST.

A point to be noted is that the scan stuck-open test sequence is independent of the circuit implementation, and as demonstrated in the next section, is amenable to a simple BIST implementation. This makes it useful for periodic testing. Other known sequences, like the checking sequences [7.3, 7.4], are dependent on the circuit implementation. They are also not amenable to a simple logic BIST implementation.

7.3 Proposed enhanced logic BIST architecture

We have so far established that flush tests, with various clock controls and carefully ordered patterns, are needed to maximize stuck-open coverage. We have also seen the rationale for maximizing coverage in the context of system testing. During manufacturing testing, if scan top-off patterns are used in conjunction with logic BIST then such patterns can be applied from the ATE. Note that during system testing the ATE is not available and we are completely reliant on the logic BIST structure to test for these

potential field failures. Thus, logic BIST needs to be augmented to apply the scan stuck-open flush test sequence.

The modified logic BIST architecture we are proposing is shown in Figure 7-3. In addition to the PRPG, possibly concatenated with a weight modifier, we need a second data source for the various flush tests. A multiplexer is included to drive the scan chains from these two data sources. Secondly, to control the clock we need a clock modifier module that will: slow the clock for half-speed test or very slow speed test, or freeze the clock at either 0 or 1 for an extended period of time. Finally, there is a BIST sequencer which controls the two data sources, the data selector, the scan clock modifier and MISR. In addition, it is responsible for starting the logic BIST operation, sequencing through the various stages of the logic BIST test session and indicating the completion of the test session.

The darkly shaded boxes are legacy logic BIST blocks and the proposed architecture builds on that. The BIST_SEQUENCER, lightly shaded in the diagram, contains the OLD_BIST_SEQUENCER. This legacy block scanned in the patterns and applied the TDF/path-delay patterns at-speed to the combinational part of the design.

We assume that this legacy sequencer generated two signals TE_OLD, FUNC_CLK_OLD to accomplish this. It used the ORIGINAL_SCAN_CLOCK and the Functional_Clock to generate these patterns. We also assume that it controls the MISR to accumulate the results, compare it with the expected results and generate the error signal. This is not shown explicitly in the diagram. The un-shaded blocks are new blocks that we will define below.

The BIST_SEQUENCER generates a set of new control signals, above and beyond those generated by the OLD_BIST_SEQUENCER. FLUSH identifies whether the sequencer is generating the scan stuck-open flush test of Table 7-1 or not. FLUSH is used to modify TE_OLD and FUNC_CLK_OLD to generate TE, FUNC_CLK as shown in Figure 7-4. The TE and FUNC_CLK signals go to the scan chains and the MISR.

FUNC is also used to select the data, going into the scan chains, either from the FLUSH_DATA_GENERATOR or the PATTERN_MODIFIER.

The BIST_SEQUENCER generates four control signals to control the SCAN_CLK_MODIFIER: NORMAL_SCAN, HALF_SCAN, PRECHARGE_1 and SLOW_CLOCK. They indicate, respectively, that the original scan_clock, half-speed scan clock, clock held to 1 and slow clock are to be generated. Note that there is no specific signal to hold the scan clock to 0. If the above four signals are set to 0 then the SCAN_CLOCK_MODIFIER will hold the scan clock to 0.

A realization of the SCAN_CLK_MODIFIER block, using the above control signals generated by the BIST_SEQUENCER, is shown in Figure 7-5. NEW_SCAN_CLK is the output of this block that drives the scan clock input of the scan chains.

The BIST_SEQUENCER generates a set of control signals to control the FLUSH_DATA_GEN: ALL_1, DATA_OO11, DATA_01. ALL_1 indicates that the flush test 11…1 is to be generated, DATA_0011 indicates that the flush test 00110011… is to be generated, and DATA_01 indicates that the flush test 0101… is to be generated. Note that we do not have any specific signal for the flush test 00…0. If the above three control signals are set to 0 then FLUSH_DATA is 0.

The above control signals are used by the FLUSH_DATA_GEN as shown in Figure 7-6. Note that a free flow of 00110011… and 0101… patterns are being generated from clock signals. HALF_FLUSH_CLK is the half-speed scan clock generated within the SCAN_CLK_MODIFIER of Figure 7-5.

A definition of the BIST_SEQUENCER that generates the various control signals is shown in Figure 7-7. We assume that on power up the state machine enters the RESET state and the following control signals are all set to 0: NORMAL_SCAN, FLUSH, HALF_SCAN, NORMAL_SCAN, PRE_CHARGE_1, SLOW_CLK, ALL_1, DATA_0011, DATA_01, LBIST_ON. We use the following notation to label the edges:

<a,b,..> / <x,y, ..> . Here a, b, before the "/", are the list of signal-value pairs that will cause the transition to occur and x, y, after the "/", are the signal-value pairs that result as a result of this transition. For example, the "START" to "APPLY 1s" occurs when LBIST_START=1 and this transition causes LBIST_ON, ALL_1, NORMAL_SCAN, FLUSH to be set to 1. We assume that all these outputs are latched outputs. In the figure, OLD_LBIST_SEQUENCER is the legacy sequencer and the new function is described independently. Once the scan stuck-open flush test is applied the sequencer relinquishes control to the legacy sequencer. This was done to explain the main contribution of this work. An actual implementation will merge the two in a more optimized form.

In the above state diagram we used the symbols K, M, N, and S which are defined in Table 7-3. With this background the state diagram of Figure 7-7 should be self-explanatory. Note that we have added a SYNC state to synchronize with the global LBIST controller and wait for it to reset the LBIST_START signal before moving on to the START state.

7.4 Conclusions

Using results obtained earlier for manufacturing tests, we discussed the shortcomings of current logic BIST structures in detecting open defects that are important in periodic field testing. Based on earlier results, we argued that if the stuck-open faults not detected by current logic BIST are left undetected, they may cause functional failures. A new set of tests to detect these faults were presented earlier. We proposed a new architecture for logic BIST that can apply these tests.

Table 7-1: Scan resistive stuck-open flush tests proposed in Chapter VI

Tests	Comments
11…1	Normal-speed flush tests in this designated order
00…0	
0011 …	
Hold clock signal at 1 for M cycles	Half-speed flush test after pre-charging clock lines to 1 (this is the modified test)
0011 …	
Hold clock signal at 0 for N cycles	Half-speed flush test after pre-charging clock lines to 0
Half-speed flush test 0101…	
Applying 01 slow for 2 cycles	Slow speed flush test

Table 7-2: Additional scan based tests described in Chapter V

D = X1, TI = 0X, TE = 10, Q = 01
D = X0, TI = 1X, TE = 10, Q = 10
D = 1X, TI = X0, TE = 01, Q = 10
D = 0X, TI = X1, TE = 01, Q = 01

Table 7-3: Parameter for BIST_SEQUENCER

K	No of scan clock cycles to fill the scan chain
M	No of scan clock cycles required to precharge clock node to 1
N	No of scan clock cycles required to precharge clock node to 0
Tslow	Period of the slow clock
Tscan	Period of the scan clock
2S	Tslow/Tscan

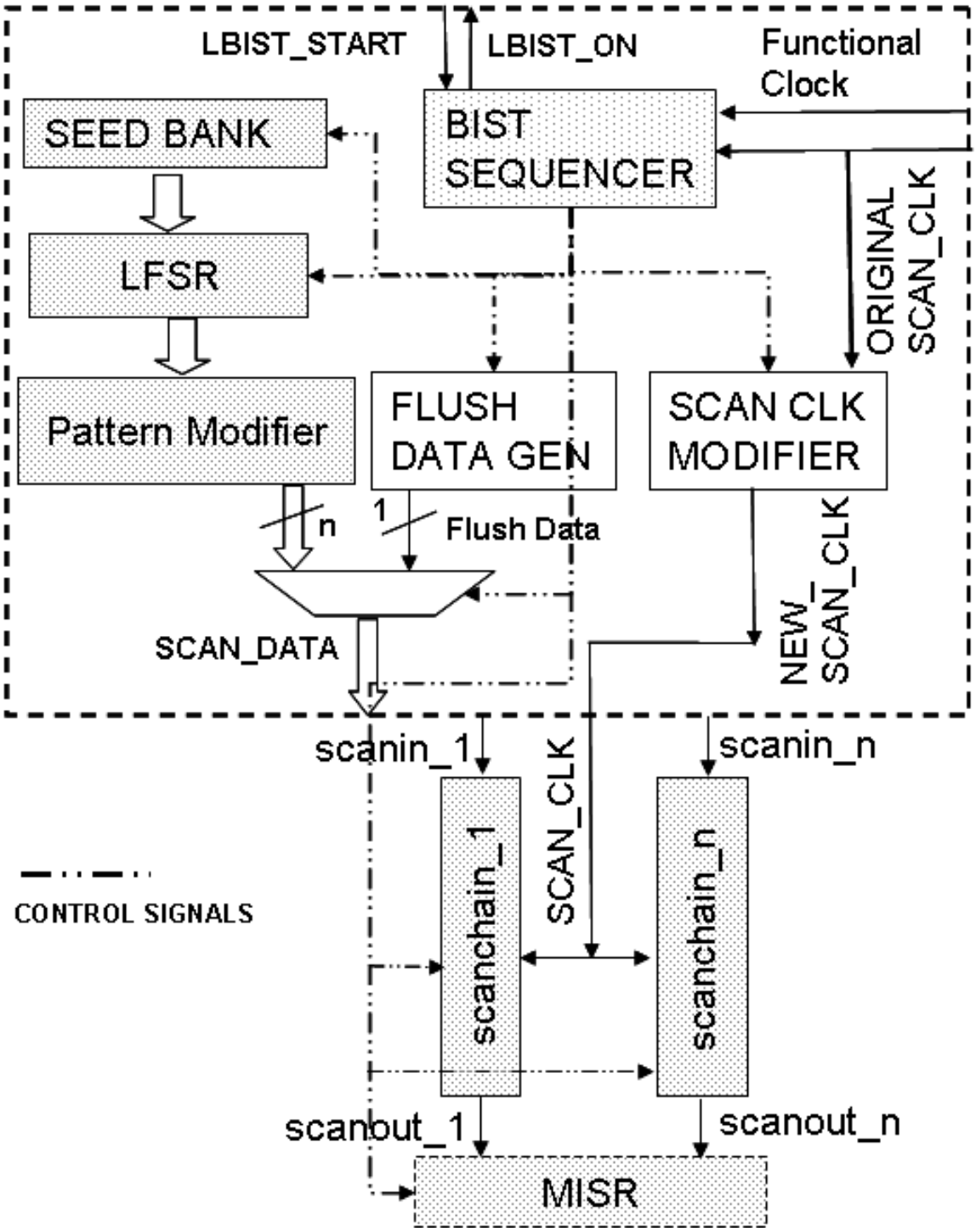


Figure 7-3: Enhanced logic BIST architecture proposed

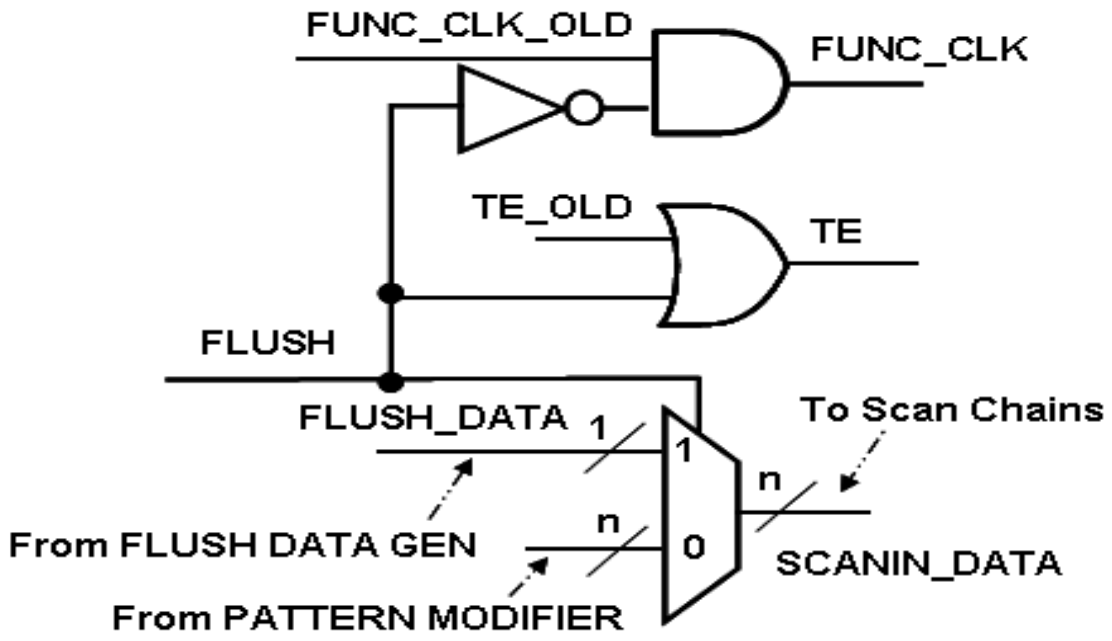


Figure 7-4: SCAN_DATA MUX and TE, FUNC_CLK generation

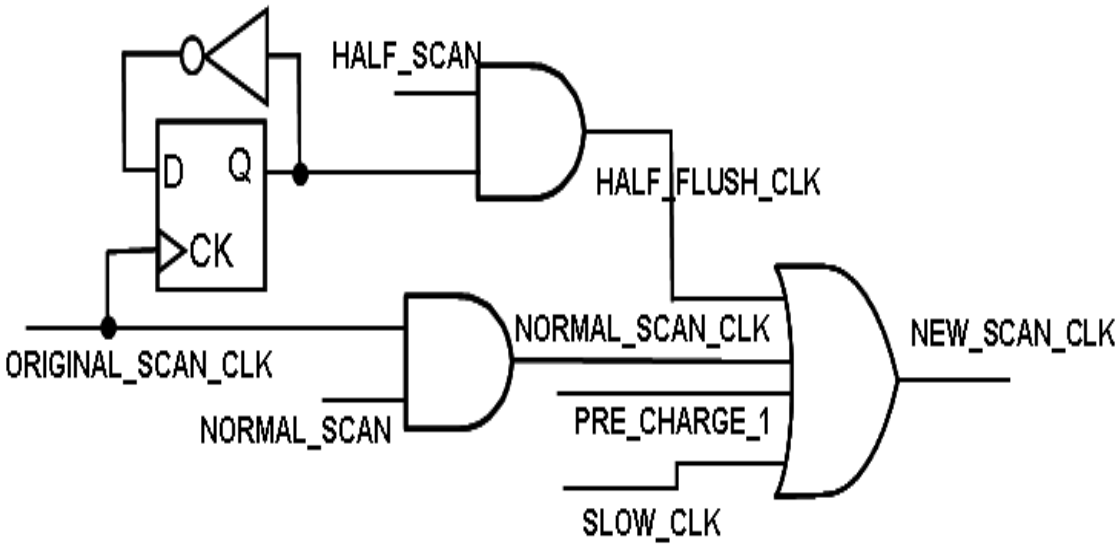


Figure 7-5: A realization of SCAN_CLK MODIFIER

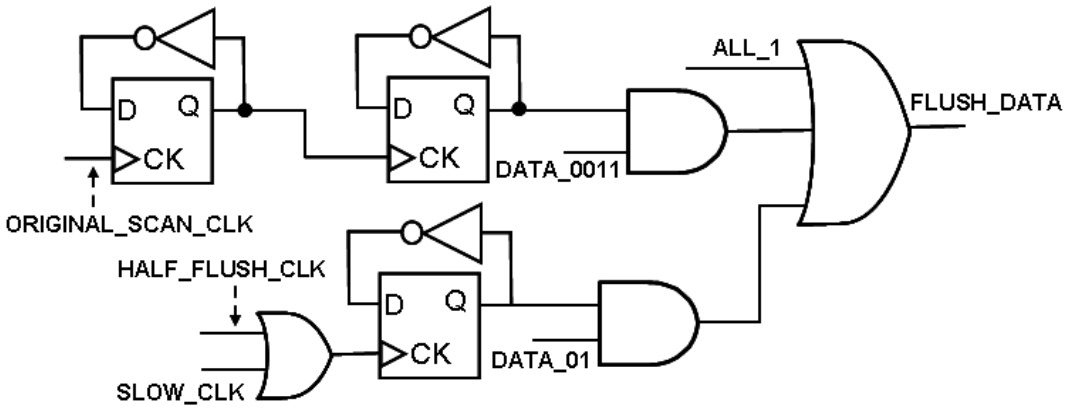


Figure 7-6: An implementation of FLUSH_DATA_GEN

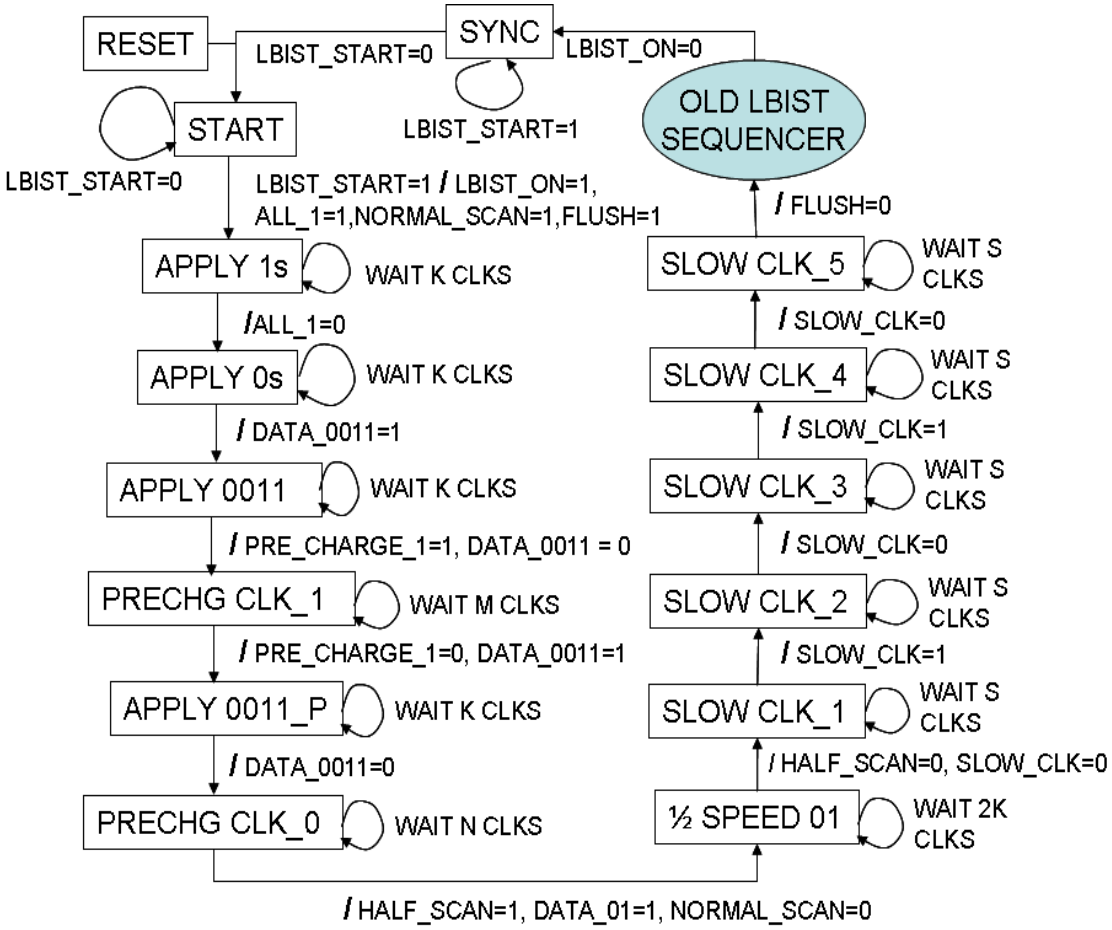


Figure 7-7: A definition of the BIST SEQUENCER

CHAPTER VIII DETECTION OF TRANSISTOR STUCK-OPEN FAULTS IN ASYNCHRONOUS INPUTS OF SCAN CELL

In the previous chapters, faults in fully-synchronous flip-flops are considered. In many designs asynchronous inputs are used to set and/or reset flip-flops. Considering a scan cell implementation used in an industrial design we show that stuck-open faults in some transistors driven by asynchronous inputs require two new flush tests. Such faults, if left undetected, cause functional failures. The two new tests increase the overall stuck-open fault coverage of each scan cell by approximately 5%. This will significantly improve the overall test quality due to the large number of scan cells contained in large industrial designs.

8.1 Introduction

In Chapter III, IV, V and VI, we investigated the detection of SAFs, SONs, bridging faults and SOPs internal to the scan chains [8.10, 8.17-8.19], respectively. All the earlier works consider fully-synchronous scan flip-flops only. In this chapter, we consider open faults in transistors driven by asynchronous set/reset inputs.

The resistive open fault model is used in this study by injecting a large resistance between the drain, source or gate of the faulty transistor and the node to which they would otherwise be connected. Two pattern tests are required for the detection of open faults [8.11]. If the resistance introduced by the open is not large, the open will cause a small delay defect [8.15]. In this chapter, we consider large resistance opens only which cause gross delay defects.

The remainder of the chapter is organized as follow. In Section 8.2, a studied asynchronous scan cell used in an industrial design is described. In addition, open faults considered in this work are also discussed. In Section 8.3, the proposed new flush tests for the detection of considered open faults are presented. Finally, this chapter is concluded in Section 8.4.

8.2 Asynchronous scan cell studied and faults considered

In Figure 8-1 we give the transistor level circuit diagram of a scan cell with asynchronous reset input used in a 90nm industrial design. In Figure 8-1**,** node D is the functional (data-in) input driven by the combinational logic and TI is the test input (scan-in) applied to the scan cell. The circuit in the dashed rectangle is the multiplexer used for selecting between D and TI. The value at node TI is selected to propagate to the scan cell output (Q) if the test enable signal (TE) is 1 and the value at D is propagated to the output by setting TE to 0. The circuit between nodes DP and MD is the master stage. The slave stage is the circuit between the output (MD) of the master stage and the scan cell output Q. Input pin CD is used to asynchronously reset the scan cell (i.e. CD asynchronously sets the output Q to 0 when CD changes to 0). We will use this scan cell for our study. However, the conclusions drawn are expected to hold for other scan cells which use asynchronous inputs.

In the scan cell of Figure 8-1, there are a total of 38 transistors. Four transistors (10.5%) N14, N04, P09 and P13 are driven by the asynchronous reset input CD. Removing these four transistors will result in a fully-synchronous flip-flop. To detect all the detectable open faults in the fully-synchronous scan cell, we have proposed a set of tests in [8.17]. No earlier work has considered the opens in the transistors driven by the asynchronous inputs to scan cells. In this chapter, we consider detection of stuck-open faults in the four transistors driven by the asynchronous reset signal CD.

Table 8-1 summarizes the results obtained in this work. The transistors driven by signal CD are of two types: (i) the P transistors are on when CD = 0 (P09 and P13); (ii) the N transistors are on when CD = 1 (N04 and N14). In Table 8-1, column 3 indicates that open faults in the transistors will affect the functional mode of operations. Columns 4 and 5 indicate that except for opens in N14 open faults in other transistors will not be detected by the standard flush tests and ATPG boundary tests. Column 6 shows that open faults in N14 are detected by the existing flush test 00110011…and opens in N04 can be

detected by the new flush test proposed in [8.17]. In this chapter, we propose two new flush tests to cover the remaining open faults in transistors P09 and P13 in Figure 8-1. Thus the two new flush tests improve the overall stuck-open fault coverage of a scan cell by 5.26%. Considering that the number of scan cells in a design can be very high [8.10], additionally detecting open faults in two transistors per scan cell can have a significant impact on the overall test quality. The same two flush tests detect the faults in all the scan cells of the design.

Table 8-1: Summary of the transistor SOPs considered

Fault Class	Faulty Transistor	Functional Failure	Existing Flush Test	ATPG SAF/TDF Boundary Test	Tests for Detection	% Weight
CD = 1	N14	Yes	Yes	No	0011..0011	2.63%
	N04	Yes	No	No	[8.17]	2.63%
CD = 0	P09	Yes	No	No	New flush test	2.63%
	P13	Yes	No	No	New flush test	2.63%

8.3 Proposed flush tests

In this section, we discuss the detection of open faults in transistors controlled by the reset signal CD. In Section 8.3.1, the proposed new flush tests for the detection of open faults in P09 and P13 are presented. In Section 8.3.2, we discuss the detection of stuck-open faults in N04 and N14.

8.3.1 Detection of opens in transistors turned on when CD = 0

Transistors P09 and P13 are turned on when CD = 0. P09 is located in the master stage and P13 is in the slave stage. In the following discussions, we present the proposed

new flush tests for the detection of opens in P09 and P13. We also discuss why standard flush tests and ATPG SAF/TDF boundary tests do not detect these faults. The impact of these faults, if left undetected, on the functional operation is also discussed. Detection of faults was ascertained using HSPICE simulation of the proposed tests on a scan chain segment of three scan cells with a fault injected into the second cell.

Consider the open faults of transistor P09 denoted by arrows in Figure 8-2. To detect the fault, we first need to initialize Q to 1 in clock cycle i. In the clock cycle i+1 we set CD to 0 and change CD back to 1 when CP = 1. This is shown in Figure 8-3(a).

We refer to Figure 8-2 and Figure 8-3 in the following discussion. In clock cycle i, output Q is initialized to 1 by setting TI = 1, TE = 1 or D = 1, TE = 0. This sets DP and S1 to 1. Since CD = 1, N14 is on. Hence, node MD is driven by VSS. When clock (CP) changes to 1, P02 and N02 are on and the value 0 at node MD is propagated into the slave stage. Q is thus set to 1 at the first rising edge of clock cycle i+1.

Next, we consider clock cycle i+1. When CP = 1 we change CD to 0 as shown in Figure 8-3(a). Note that in order to avoid holding time violation CD needs to be changed to 0 after the required hold time. This will turn on P09 and turn off N14 in the fault-free circuit. The node MD is then driven by VDD through transistor P09. The value 1 propagates to the slave stage since N02 and P02 are on when CP = 1. Thus the output Q changes to 0 in the fault-free circuit. Meanwhile, node S1 is set to 0 since MD = 1 turns on N08 and N07 when CP = 1. CD is then changed back to 1 before CP changes to 0 (cf. Figure 8-3(a)). This turns on N14 and turns P09 off. In the fault-free circuit, the node MD retains the value 1 since S1= 0 turns P14 on. Therefore nodes SD and Q retain the values 1 and 0 within CP = 1, respectively. When CP changes to 0, P02 and N02 are off. Although CD = 1 turns off P13, SD = 1 sets the node S8 to 1 and turns on P04. Therefore the output Q still retains the value 0 in the rest of the clock cycle i+1. The solid lines in Figure 8-3(a) show the waveforms of CP, CD and Q in the fault-free circuit. However, in the faulty circuit, changing CD to 0 when CP = 1 turns off N14 and node MD will be

floating due to the open fault in P09. Besides, P13 is on and N04 is off since CD = 0. Since CP = 1 turns off P03, CD = 0 will not change the value at node SD. Hence, in the faulty circuit, nodes MD, SD, S8 and Q retain the values 0, 0, 1 and 1, respectively. Since CD is changed back to 1, which turns off P13 before CP changes to 0, the output Q retains the value 1 which is faulty at the next rising edge of the clock. The waveform of Q for the faulty circuit is shown in dashed lines in Figure 8-3(a).

It is important to note that if CD is changed back to 1 after the falling edge in cycle i+1, as shown in Figure 8-3(b), the faulty value 1 will not be observed at the rising edge of the subsequent cycle. This is explained next. When CP changes to 0, transistors P03 and N03 are turned on while P02 and N02 are turned off. The node SD is driven by VDD through transistors P03 and P13 since CD is 0. Hence, the output Q changes to 0 at the falling edge instead of changing simultaneously when CD changes to 0. Thus, we will not observe the faulty value at the rising edge of the next clock cycle. Therefore, the open fault in transistor P09 will not be detected. The fault-free and faulty waveforms are shown in Figure 8-3(b) in solid and dashed lines, respectively.

To accomplish the detection of this fault, we propose a new flush test called *master reset transistor flush test* discussed next. The test scans in all ones (11…1) into the scan chain with CD = 1. This helps to initialize the output of the scan cells in the scan chain to 1. Then the test applies the values TI = 1, D = X, TE = 1 for one clock cycle toggling CD to 0 and back to 1 within CP = 1 duration. This is shown in the waveform of CD in clock cycle i+1 in Figure 8-3(a). Finally, the output values stored in the scan cells are shifted out to compare with the expected values. Note that the open resistance is assumed large enough such that P09 is not turned on in the duration of toggling CD to 0 shown in Figure 8-3.

Next, we discuss the detection of open faults in P13 shown in Figure 8-4. We propose another flush test called *slave reset transistor flush test*. Again, the 11...1 sequence is scanned into the scan chain to initialize the outputs of the scan cells. This is

followed by the values TI = 1, D = X, TE = 1 and toggling CD to 0 and back to 1 within CP = 0 phase as shown in the waveform of CD of Figure 8-5(a). The detection of this fault is shown in Figure 8-5(a) by the faulty value 1 observed at the rising edge of clock cycle i+2. From Figure 8-5(b), we can also see that changing CD back to 1 across the clock phases (changing CD back to 1 after the next rising edge) still detects the fault. However, this will introduce additional test cycles. Therefore, we toggle CD within CP = 0 in order to minimize the testing time. Again, we note that the open resistance is assumed to be large enough such that P13 is not turned on during CD = 0 shown in Figure 8-5.

We have seen that in order to detect the open faults of transistors P09 and P13, we need to set CD to 0. However, when applying the standard flush tests and ATPG boundary tests targeting TDFs at inputs TI, TE, D and output Q, CD is held at 1.

Since detection of open faults requires two pattern tests, the boundary TDF test at CD is the only other possible choice. We investigated this option. We found that ATPG boundary tests targeting transition delay faults at CD do not provide the detection of these faults. The ATPG tools model the scan cell as a black box. The test patterns targeting CD slow-to-fall can initialize the scan cell to 1 by applying TE = 0, D = 1, TI = X. However, the slow-to-fall fault at CD does not model the SOPs in transistors P09 and P13 properly. The test computed by existing ATPG tools holds CD at 0 for both clock phases (CP = 1 and CP = 0) in the second test pattern. Hence, they do not ensure that CD changes within CP = 1 or CP = 0 as discussed above. Therefore, the ATPG tests do not detect these SOPs.

To have the ATPG generate tests to detect these faults, controlling the timing of the change in signal CD is required. This can potentially lead to additional tests for each scan cell. The proposed flush tests have the advantage that all the SOPs in transistors driven by CD in the scan cells are detected by the same two flush tests.

It is important to note that the open faults in the transistor P09 will result in errors during the functional mode of operation. Five possible cases may happen when trying to asynchronously reset the scan cell in clock cycle i+1. They are shown in Figure 8-6 as waveforms CD1, CD2, CD3, CD4 and CD5, respectively. In case 1 the asynchronous reset pulse occurs when CP = 1. The output of the scan cell will not be set to 0 in the faulty circuit. Thus, it results in functional failure. When the asynchronous reset pulse is over a time greater than half the clock cycle as in CD2, the scan cell output will not set to 0 until the falling edge. This will lead to a delay and a functional failure may occur if the scan cell is connected to a negative edge triggered flip-flop. In the third case CD3 changes back to 1 in clock cycle i+2. This results in the same errors as in the case of CD2. Finally, no functional error occurs in the case of CD4 and CD5 where CD changes when CP = 0 since the output will be reset using P13.

Similarly, for the stuck-open faults in P13, if left undetected, it will introduce a delay in the affected scan cell, which may lead to functional failure as in CD4 and CD5 shown in Figure 8-6. In the cases of CD1, CD2 and CD3 no functional errors occur since the output will be reset using P09. Therefore, it is important to detect the open faults in P09 and P13 as they may lead to functional failures if left undetected.

8.3.2 Detection of opens in transistors turned on when CD = 1

Similar to the case of transistors P09 and P13 discussed in Section 8.3.1, one of the transistors in this case, N14, is in the master stage and the other N04 is located in the slave stage.

Figure 8-7 shows the master and slave stages with stuck-open faults in transistor N14 denoted by the arrows. Assume that DP = 1 is propagated into the master stage when CP = 0. Node S1 is set to 1 and turns on transistor N09. In the fault-free circuit, MD is driven by VSS through N14 with CD = 1. However, MD will not be set to 0 due to the

open fault in transistor N14. Therefore, the output Q can never be set to 1 in the faulty circuit. These open faults are detected by the standard flush test 0011…0011 with CD = 1.

In functional mode of operation, if left undetected, these faults will result in errors when the value 1 on D attempts to propagate to output Q.

Next, consider the open faults in the transistor N04 highlighted by arrows in Figure 8-8. To detect these faults, we apply TI = 1. The node MD is set 0 when CP = 0 and the value 0 propagates to the node SD when CP changes to 1. Hence, the transistors P05 and P12 are turned on. When CP changes to 0 SD is driven by VSS through the transistors N04 and N13. Thus, in the fault-free circuit the output Q is set to 1 at the rising edge and retains the value for one clock cycle. However, in the faulty circuit when CP changes to 0 the node SD is floating due to the open fault in N04. If we wait for a long enough time, the node S8 will discharge to 0 and turn on P04. The output is thus set to 0 which is faulty. These faults can be detected by applying the flush test at very slow speed. We proposed such tests in [8.17].

8.4 Conclusions

We investigated the detection of stuck-open faults in transistors driven by an asynchronous reset input in a scan flip-flop. We found that the existing flush tests and ATPG tests targeting inputs and outputs of the scan cell do not detect the open faults in the transistors which are used to reset the scan cell. To detect these faults, we proposed two new flush tests which improve the total open fault coverage by over 5%. In addition, we showed that these faults can lead to failures in the functional mode of operation if left undetected. Therefore, it is important to detect them. The two new flush tests together with the tests we proposed earlier in [8.17] detect all the detectable large resistance stuck-open faults in a scan cell with asynchronous inputs.

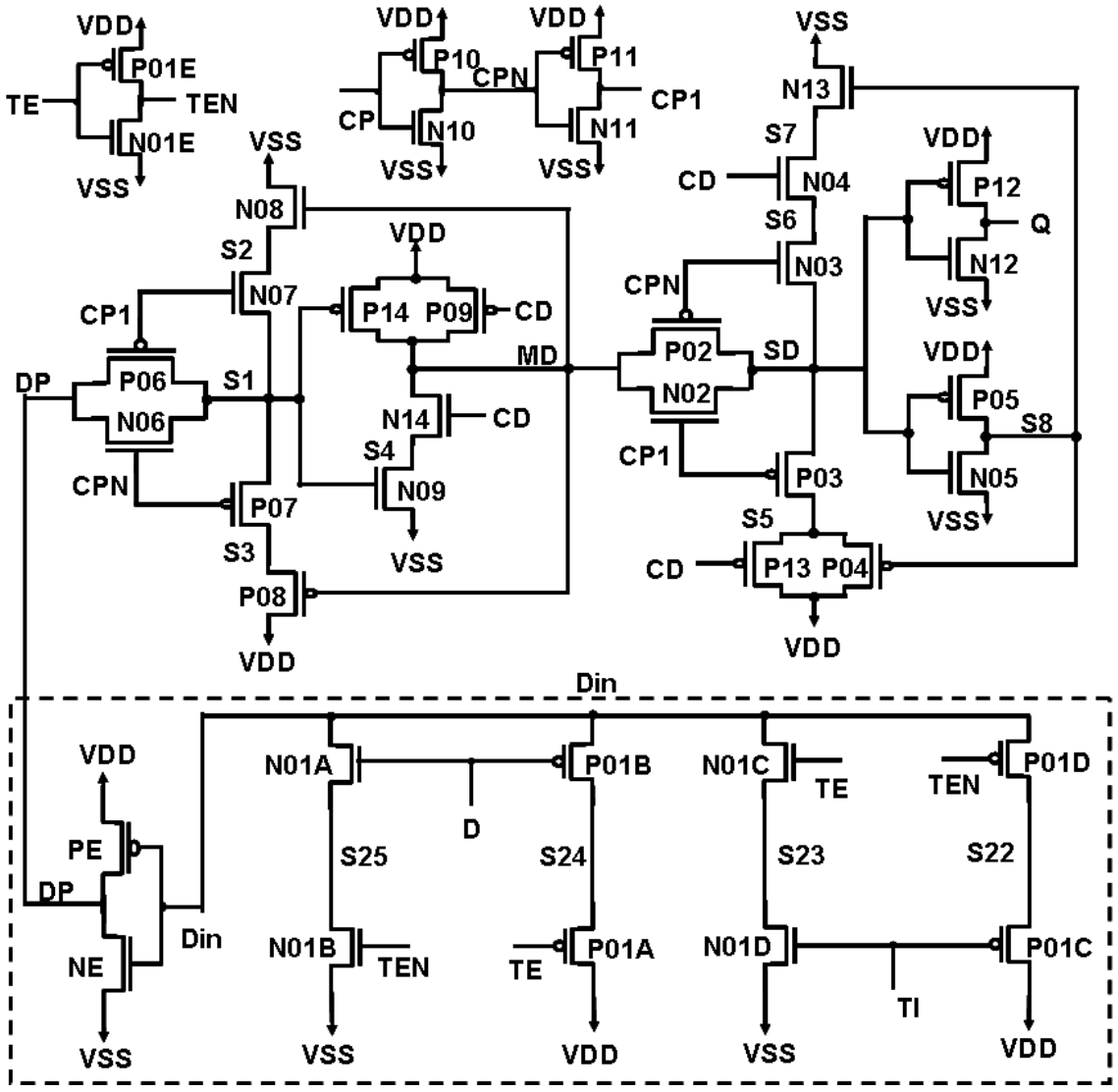


Figure 8-1: Scan cell with asynchronous reset input CD

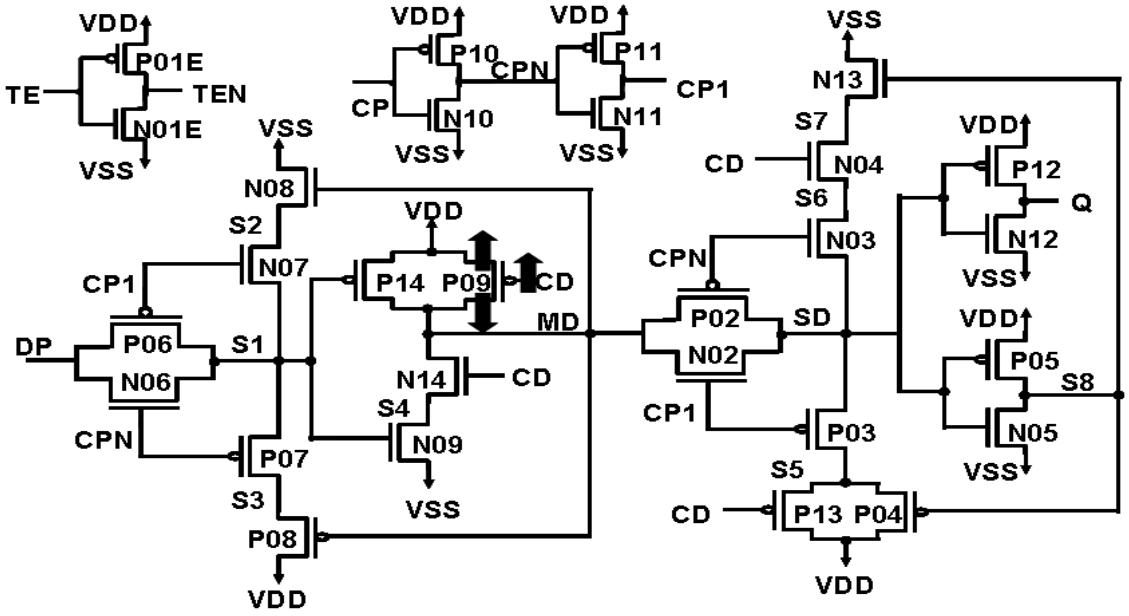


Figure 8-2: SOPs in transistor P09

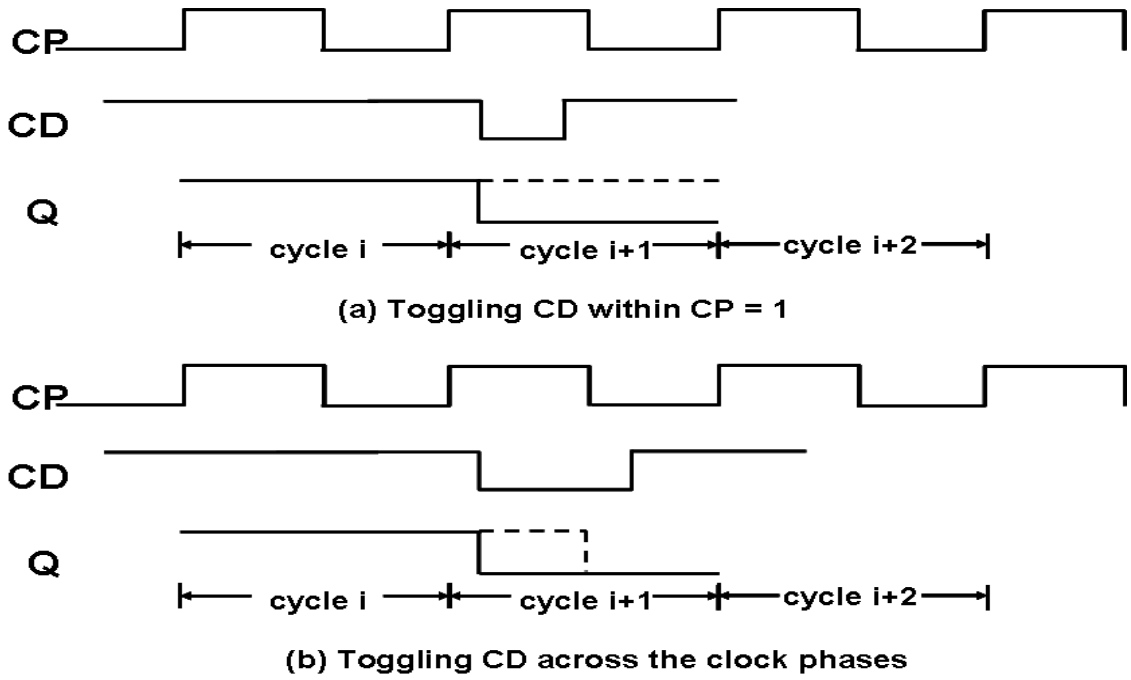


Figure 8-3: Detection of SOPs in transistor P09

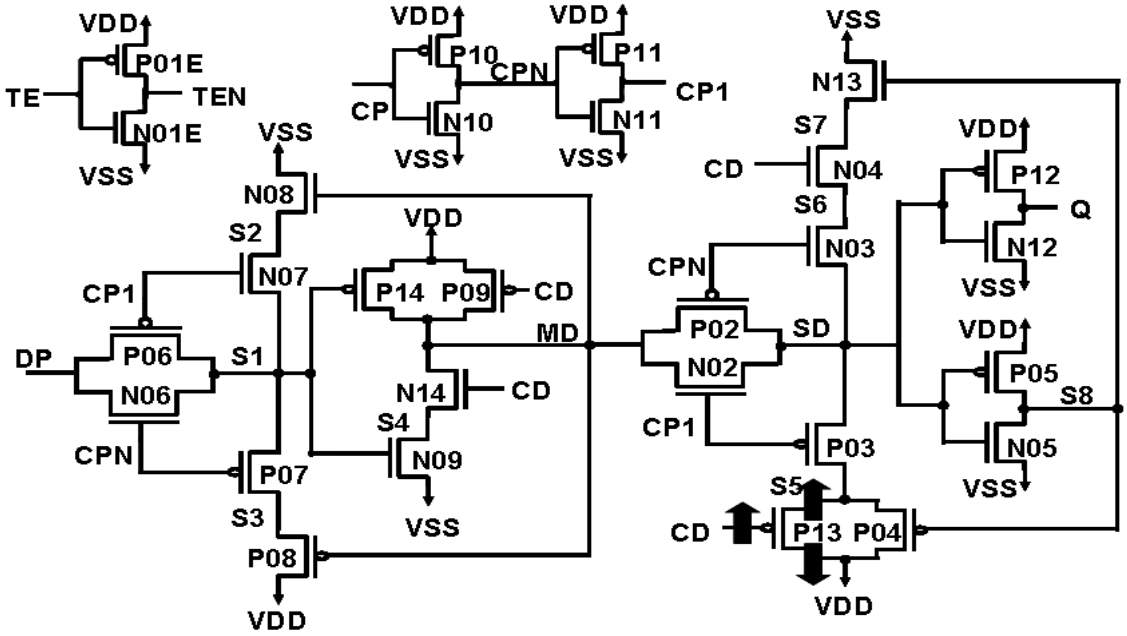


Figure 8-4: SOPs in transistor P13

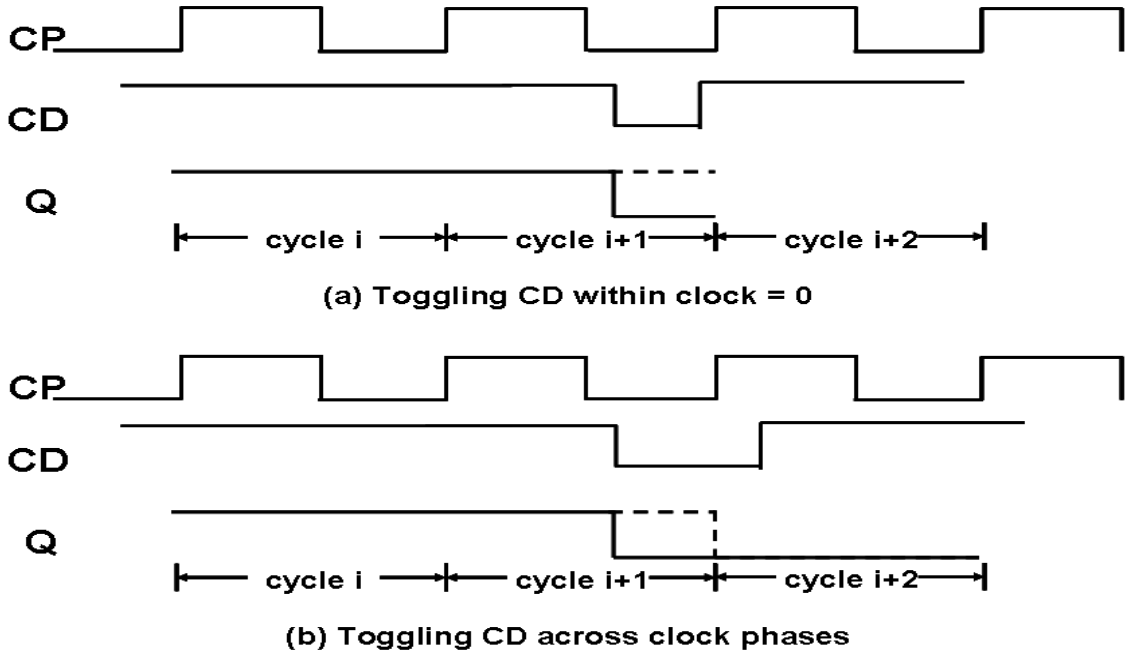


Figure 8-5: Detection of SOPs in transistor P13

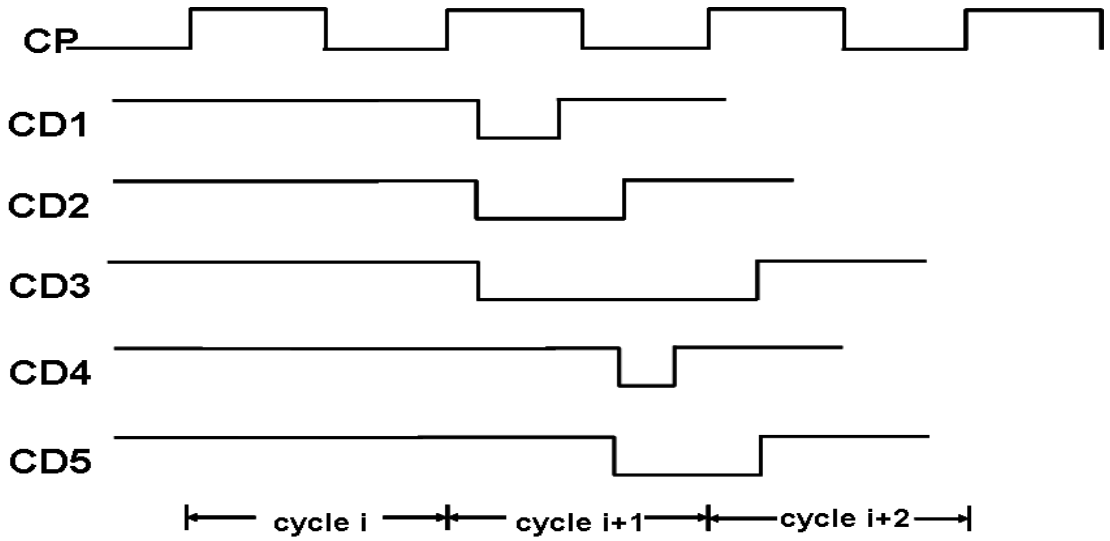


Figure 8-6: Cases of CD reset in functional mode of operation

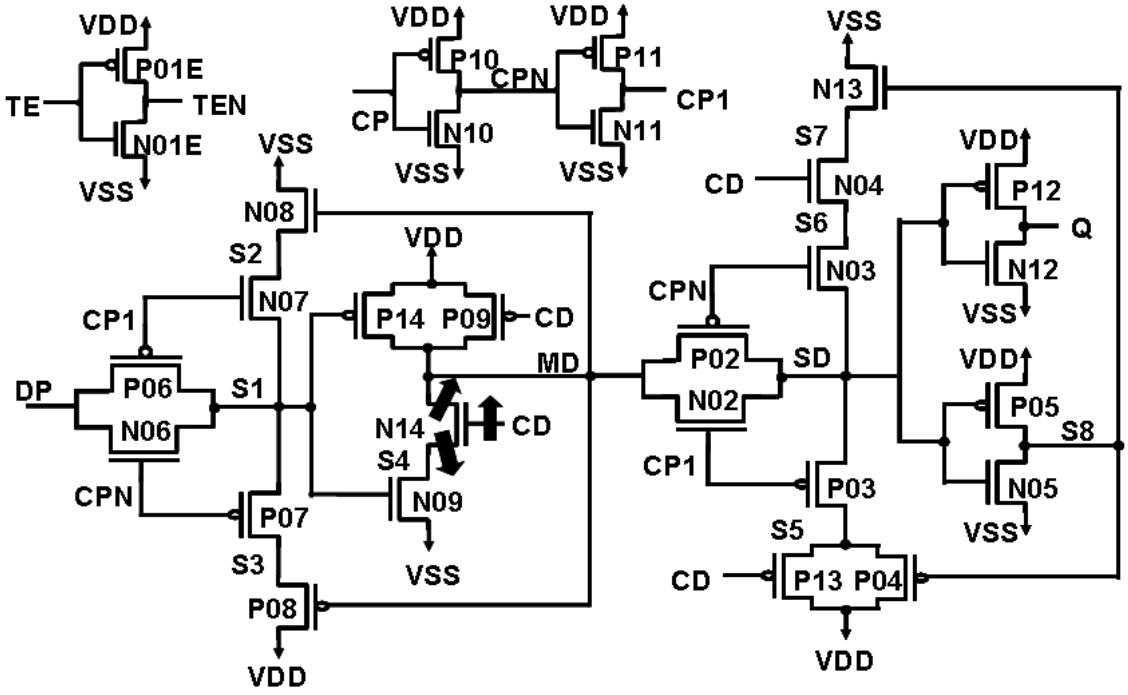


Figure 8-7: SOPs in transistor N14

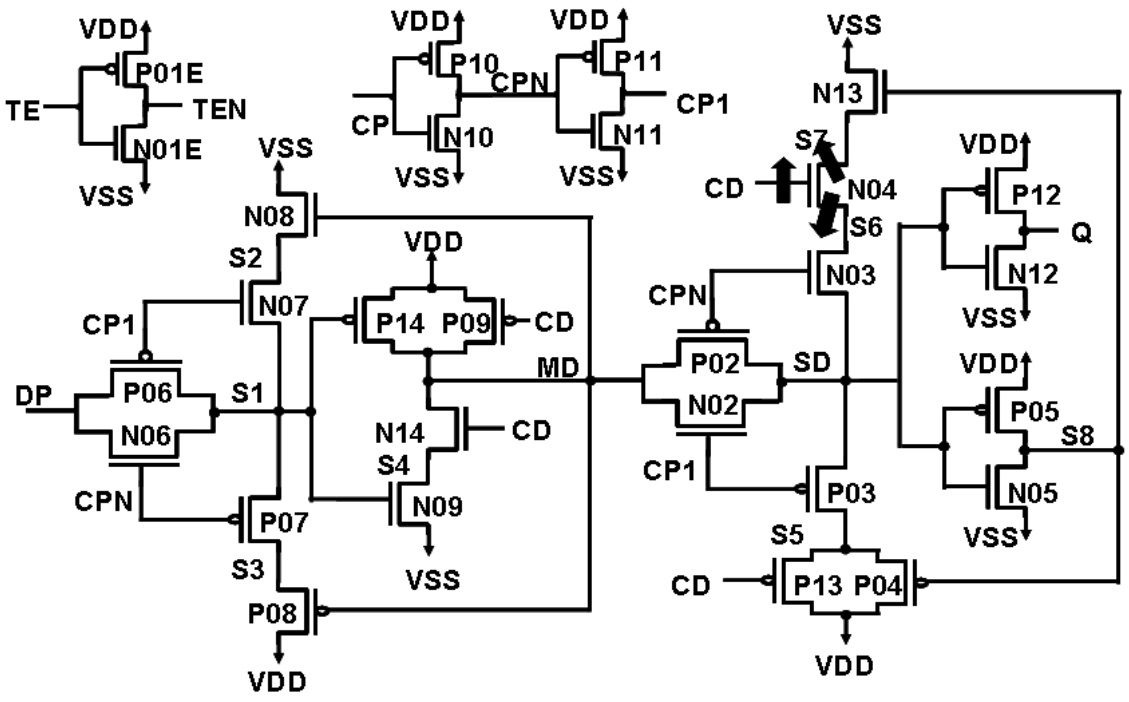


Figure 8-8: SOPs in transistor N04

CHAPTER IX CONCLUSIONS

In scan designs, all flip-flops in the logic part of a design are grouped into the scan chains that facilitate loading tests applied to detect defects as well as observing the circuit response to the tests. Industrial data shows that nearly half of the transistors in the logic parts of large VLSI designs typically reside inside scan cells [9.1, 9.2]. Even though the main purpose of scan cells is to facilitate loading tests and unloading test responses, faults in scan cells may affect functional operation if left undetected. The undetected faults in scan cells may also affect long term reliability of shipped products. Nevertheless, current test generation procedures do not directly target faults internal to the scan cells.

The main objective of this thesis is to improve the detectability of scan cell internal faults by new cost effective tests and test methods. A comprehensive investigation on faults internal to scan cells using typical fault models is developed.

First, in chapter III, we investigated the use of standard scan cells and existing methods of generation and application of scan based tests to detect scan cell internal faults. Stuck-at and stuck-on fault models are applied for the investigation. We also proposed a new test called half-speed flush test to cover cell internal faults to similar degree as the checking sequence based tests in [9.3, 9.4]. Experiment results on a standard scan cell used in a 90nm industrial design show that the new flush test increases stuck-at fault coverage by 2.3% for a cell and by 1.03% for the full-chip. Given that today's designs attempt to achieve over 99% coverage this increase is quite significant. Coverage gaps are identified and investigated. We showed that there is also a large class of IDDQ only detectable faults that poses a serious reliability risk while IDDQ testing may not be feasible for 90nm and beyond.

In Chapter IV we investigated detection of a set of scan cell internal bridging faults extracted from layout. We showed that the detection of some zero-resistance non-

feedback bridging faults requires two-pattern tests. Half-speed flush tests proposed to detect stuck-at and stuck-on faults also detect additional bridging faults. We classified the undetectable faults based on the reasons for their undetectability. We observed that the driver strengths of the scan cell inputs can be optimized to improve the bridging fault coverage. Both zero-resistance and nonzero-resistance bridging fault models are considered in this work. A low power supply voltage based test method and IDDQ testing are examined for resistive bridging fault detection.

In Chapter V we considered large resistance open faults in transistors internal to scan cells. It showed that existing tests miss many open faults. Analysis shows that detection of some opens require proper initial conditions applied to faulty nodes. This is can be done by ordering the traditional flush tests. We also observe that detection of some opens requires specific initial state of clock signal before applying flush tests. In order to satisfy these conditions, we proposed to hold the clock signals for a length of time before applying flush tests. Besides, very slow speed test is shown necessary to detect additional faults. According to the observations a new set of flush tests called scan stuck-open flush tests is proposed to greatly enhance the coverage of large resistance opens. In addition, a new set of ATPG generated tests was also presented. Together, these tests are shown to achieve the maximum possible coverage of large resistance opens in transistors internal to scan cells.

Chapter V considered large resistance opens internal to scan cells. In Chapter VI, it showed that the fault coverage drops significantly when opens with moderate resistances are considered. The open faults are classified into 7 classes based on the tests in Chapter V assuming the large open resistance. Earlier scan stuck-open flush tests are modified to detect a class of open faults with wider resistance range. In addition, leakage current effects are considered. We found that the increased leakage currents due to higher testing temperature will widen the detectable resistance range of a class of internal opens. Finally, we observe that the ATPG boundary TDF tests detect smaller resistance opens

than the flush tests for a class of faults by taking advantage of the delays in the combinational logic.

Logic BIST is commonly used for online and periodic testing is to identify defects, like opens, resulting from the wear and tear of the circuit. Based on earlier investigations in Chapter V and Chapter VI, a novel Logic BIST architecture to implement the new set of flush tests to detect open defects is proposed in Chapter VII.

As mentioned earlier, the conclusions drawn from the studied scan cell can be easily extended to other implementations of scan cells. In Chapter VIII, an asynchronous scan cell with a reset input is studied. Two new flush tests called slave reset transistor flush test and master reset transistor flush test are added to the tests described in Chapter V and Chapter VI. Such tests help to detect stuck-open faults in transistors driven by an asynchronous reset signal in a scan flip-flop.

9.1 Future research on further improving the test quality for scan cell internal faults

In our completed research described in Chapter V we studied large resistance opens internal to scan cells and showed that the additional coverage due to the new tests drops significantly when opens with moderate resistances are considered in Chapter VI. Modifying the proposed flush tests and applying tests at higher temperatures are also discussed. However, the fault coverage is still in an unacceptable range for lower open resistances. Other methods to maximize the range of detectable open resistance can improve the test quality for opens in scan cells.

In addition to opens with moderate resistances, we have mentioned in Chapter IV that the bridging fault coverage drops to an unacceptable percentage when the bridge resistance increases. We have studied IDDQ testing and low power supply method to detect larger resistance bridging faults. However, they were found to be not feasible for alleviating the coverage loss due to the bridge resistance increase. Other cost-effective

methods to improve the fault coverage of resistive bridging faults internal to scan cells should be investigated.

We have investigated the detectability of stuck-on faults within scan cells. About half of the SONs are IDDQ detectable only. However, it was shown that IDDQ testing may not be feasible for the 90nm or beyond. Investigations on these faults and developing methods to cover these coverage gaps would bring significant contributions to the reliability of circuits.

9.2 Future research to generalize the test method for all types of scan cells

We have investigated the detection of internal faults of a fully-synchronous positive edge triggered MD flip-flop and a scan flip-flops with asynchronous set/reset inputs. We derived some general rules from the previous study such as requirement of initialization of all scan cell internal nodes (including clocks, inputs and outputs) before applying test. In addition, slow speed test is also required since all scan flip-flops have the structure to retain the value from previous clock phase.

To contribute to the quality of tests for scan chain internal faults in industrial products, generalizing the test methods and automate the generation of tests for all types of scan cells in the cell libraries used in industrial designs is needed.

9.3 Silicon experiment and scan chain internal fault diagnosis

After finalizing the test set for scan cells, silicon experiment of applying the new tests to industrial products to measure the contributions of the new test methodology will be a great supplement to this thesis.

Scan chain fault diagnosis is the process of identifying the defective scan cell in a scan chain. The investigations we showed in this thesis also give some suggestions to scan chain diagnosis and could be studied in the future.

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